

REMARKS

The Official Action dated February 7, 2007 has been received and its contents carefully noted. In view thereof, submitted concurrently herewith is a Verified Translation of Applicants' Priority Document, namely Japanese Application No. 2000-080242 to which Applicants have properly claimed priority. With the filing of such a verified translation, it is respectfully submitted that the Applicants' claimed invention is entitled to an effective filing date of March 22, 2000. As previously, claims 1-6 are presently pending in the instant application.

Initially, Applicants acknowledge the Examiner's indication on page 3 of the Office Action that claims 2 and 3 have been objected to as being dependent upon a base claim but would be allowable if rewritten in independent form including all the limitations of the base claim and any intervening claims. In this regard with the submission of a verified translation of Applicants' priority document, it is respectfully submitted that independent claim 1 and thus claims 2 and 3 are now in proper condition for allowance.

Turning now to paragraphs 2 and 3 of the Office Action, claims 1-6 have been rejected under 35 U.S.C. §102(e) as being anticipated by Japanese Patent Application No. 2000-164926 A to Kawai. This rejection is respectfully traversed in that the teachings of the Japanese application are not available to the Examiner as prior art for the reasons discussed hereinbelow.

Initially, it is noted that claims 2 and 3 are included in the rejection under 35 U.S.C. §102(e) as being anticipated by Kawai; however, such claims have been indicated as being allowable over the prior art of record in paragraph 4 of the Office Action. This inconsistency, however, is deemed moot in view of the submission of a verified translation of Applicants'

priority document as well as the Examiner's specific discussion of only claims 1, 4, 5 and 6 in paragraph 3 of the Office Action.

That is, as noted hereinabove, filed concurrently herewith is a verified translation of Applicants' priority document namely, Japanese Patent Application No. 2000-080242 which was placed on file in the Japanese Patent Office on March 22, 2000 and to which the present application properly claims priority. Accordingly, it is respectfully submitted that Applicants' claimed invention is entitled to an effective filing date of March 22, 2000 which predates the June 16, 2000 publication date of the Japanese Patent Publication to Kawai. Accordingly, it is respectfully submitted that the teachings of Kawai are not available as prior art to the Examiner and thus further discussion with respect to the merits of the rejection under 35 U.S.C. §102(e) as being anticipated by Kawai is no longer believed to be warranted.

Therefore, in view of the foregoing it is respectfully requested that the objection and rejection of record be reconsidered and withdrawn by the Examiner, that claims 1-6 be allowed and that the application be passed to issue.

Should the Examiner believe a conference would be of benefit in expediting the prosecution of the instant application, he is hereby invited to telephone counsel to arrange such a conference.

Respectfully submitted,



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IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Patent Application of:)
Katsunori NISHII et al.) Group Art Unit: 2823
Serial No. 09/813,304) Examiner: Fernando L. Toledo
Filed: 03/21/2001) Confirmation No. 1540
For: SEMICONDUCTOR DEVICE AND) Date: May 4, 2007
METHOD OF FABRICATING THE)
SAME)

TRANSMITTAL OF VERIFIED ENGLISH
TRANSLATION OF PRIORITY DOCUMENT


Mail Stop Non Fee Amendment
Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Sir:

Filed concurrently with the Request for Reconsideration submitted on May 3, 2007, submitted herewith is an English Translation of Japanese Patent Application No. 2000-080242 with Declaration. Consideration is respectfully requested.

Acknowledgment is respectfully requested.

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DECLARATION

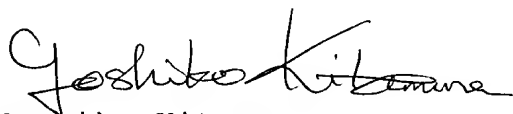
I, the undersigned, of 17-15 Shinmachi, Kaizuka-shi, Osaka, Japan, hereby certify that I am well acquainted with the English and Japanese languages, that I am an experienced translator for patent matter, and that the attached document is a true English translation of

Japanese Patent Application No. **2000-080242**

that was filed in Japanese.

I declare that all statements made herein of my own knowledge are true, that all statements on information and belief are believed to be true, and that these statements were made with the knowledge that willful false statements and the like so made are punishable by fine or imprisonment, or both, under Section 1001 of Title 18 of the United States Code.

Signature:


Yoshiko Kitamura

Dated: April 19, 2007



[Name of the Document] SPECIFICATION

[Title of the Invention] SEMICONDUCTOR DEVICE AND METHOD
OF FABRICATING THE SAME

[Claims]

5 [Claim 1] A semiconductor device comprising:

an active region formed on a substrate from a group III
nitride semiconductor; and

an insulating oxide film formed in a peripheral portion
of said active region on said substrate by oxidizing said
10 group III nitride semiconductor.

[Claim 2] The semiconductor device of Claim 1 further
comprising:

an ohmic electrode formed on said active region; and
a gate electrode formed to extend from said active
15 region onto said insulating oxide film.

[Claim 3] A plurality of semiconductor devices comprising:

a group III nitride semiconductor formed in a plurality
of device formation regions each surrounded with a scribe
region on a substrate in a wafer state; and

20 a protection oxide film formed in a peripheral portion
of said scribe region on said substrate by oxidizing said
group III nitride semiconductor.

[Claim 4] A semiconductor device comprising:

an active region formed on a substrate from a group III
25 nitride semiconductor; and

a pad electrode formed on said substrate and electrically connected to said active region; and

an insulating oxide film formed between said substrate and said pad electrode by oxidizing a group III nitride semiconductor.

[Claim 5] A semiconductor device comprising:

a laser structure formed on a substrate and having a cavity including a plurality of group III nitride semiconductors; and

a protection oxide film formed on side faces of said laser structure including facets of said cavity by oxidizing said group III nitride semiconductors.

[Claim 6] A method of fabricating a semiconductor device comprising:

a semiconductor layer forming step of forming a group III nitride semiconductor layer on a substrate;

a protection film forming step of forming, on said group III nitride semiconductor layer, a protection film for covering an active region of said group III nitride semiconductor layer;

an oxide film forming step of forming, in a region on said substrate excluding said active region, an insulating oxide film by oxidizing said group III nitride semiconductor layer with said protection film used as a mask; and

an active region exposing step of exposing said active

region by removing said protection film.

[Claim 7] The method of fabricating a semiconductor device of Claim 6, further comprising, after said active region exposing step:

5 an ohmic electrode forming step of forming an ohmic electrode on said active region; and

a gate electrode forming step of forming, on said active region, a gate electrode extending onto said insulating oxide film.

10 [Claim 8] The method of fabricating a semiconductor device of Claim 6 or 7, further comprising, between said semiconductor layer forming step and said protection film forming step, an ammonia treatment step of exposing said group III nitride semiconductor laser to ammonia.

15 [Claim 9] The method of fabricating a semiconductor device of Claim 8,

wherein said ammonia treatment step includes a sub-step of changing said ammonia into plasma.

[Claim 10] A method of fabricating a semiconductor device
20 comprising:

a semiconductor layer forming step of forming a group III nitride semiconductor layer on a substrate in a wafer state;

a region setting step of setting, in said group III
25 nitride semiconductor layer, a plurality of device formation

regions where devices are to be formed on said group III nitride semiconductor layer and a scribe region for use in dividing said substrate into chips respectively including said device formation regions;

5 a protection film forming step of forming, on said scribe region, a protection film for covering said scribe region; and

 an oxide film forming step of forming, in a region on sides of said scribe region on said substrate, a protection
10 oxide film by oxidizing said group III nitride semiconductor layer with said protection film used as a mask.

[Claim 11] The method of fabricating a semiconductor device of any one of Claims 6 to 10,

 wherein said protection film is formed from silicon,
15 silicon oxide or silicon nitride.

[Claim 12] A method of fabricating a semiconductor device comprising:

 a semiconductor layer forming step of forming a group III nitride semiconductor layer on a substrate;

20 a region setting step of setting, in said group III nitride semiconductor layer, a device formation region where a device is to be formed on said group III nitride semiconductor layer and a pad electrode formation region for external connection of said device to be formed in said
25 device formation region;

a protection film forming step of forming a protection film covering a region on said group III nitride semiconductor layer excluding said pad electrode formation region;

5 an oxide film forming step of forming an insulating oxide film in said pad electrode formation region on said substrate by oxidizing said group III nitride semiconductor layer with said protection film used as a mask; and

a step of forming a pad electrode on said insulating
10 oxide film.

[Claim 13] The method of fabricating a semiconductor device of Claim 6, 10 or 12,

wherein said oxide film forming step includes a sub-step of conducting a thermal treatment on said group III
15 nitride semiconductor layer in an oxygen ambient.

[Claim 14] The method of fabricating a semiconductor device of Claim 6, 10 or 12,

wherein said oxide film forming step includes a sub-step of conducting a thermal treatment on said group III
20 nitride semiconductor layer with oxygen ions implanted.

[Claim 15] A method of fabricating a semiconductor device comprising:

a laser structure forming step of forming, on a substrate, a laser structure having a cavity and including a
25 plurality of group III nitride semiconductors by forming said

plurality of group III nitride semiconductor layers;

a step of exposing facets of said cavity of said laser structure; and

an oxide film forming step of forming a protection
5 oxide film on said facets by oxidizing side faces of said laser structure including said facets.

[Claim 16] The method of fabricating a semiconductor device of Claim 15,

wherein said oxide film forming step includes a sub-
10 step of conducting a thermal treatment on said group III nitride semiconductor layers in an oxygen ambient.

[Detailed Description of the Invention]

[0001]

[Field of the Invention]

15 The present invention relates to a semiconductor device including a group III nitride semiconductor represented by a general formula, $\text{In}_x\text{Al}_y\text{Ga}_{1-x-y}\text{N}$ (wherein $0 \leq x \leq 1$, $0 \leq y \leq 1$ and $0 \leq x + y \leq 1$), and more particularly, it relates to a semiconductor device including an oxide film formed by
20 oxidizing a group III nitride semiconductor.

[0002]

[Prior Art]

A group III nitride semiconductor having a composition of $\text{In}_x\text{Al}_y\text{Ga}_{1-x-y}\text{N}$, that is, the so-called gallium nitride-based
25 (GaN-based) compound semiconductor, is regarded as a

promising material for a light emitting device such as an LED and a semiconductor laser diode because the interband transition of electrons is direct transition therein and its band gap is varied in a wide range between 1.95 eV and 6 eV.

5 [0003]

Recently, particularly in order to realize higher density and higher integration of information processing equipment, semiconductor laser diodes capable of outputting light of a wavelength in a blue-violet region are earnestly developed. Also, since GaN has high breakdown field, high thermal conductivity and a high electron saturation velocity, it is a promising material also for a high frequency power device. In particular, a heterojunction structure including aluminum gallium nitride (AlGa_N) and gallium nitride (Ga_N) has an electron velocity twice as large as that of gallium arsenide (GaAs) at high electric field as high as 1×10^5 V/cm to realize down sizing, and hence is expected a high frequency operation of a device.

[0004]

20 Since a group III nitride semiconductor exhibits an n-type characteristic when doped with an n-type dopant including a group IV element such as silicon (Si) and germanium (Ge), application to a field effect transistor (FET) is now under development. Also, since a group III
25 nitride semiconductor exhibits a p-type characteristic when

doped with a p-type dopant including a group III element such as magnesium (Mg), barium (Ba) and calcium (Ca), application to an LED and a semiconductor laser diode including a pn-junction structure of a p-type semiconductor and an n-type semiconductor is now under development. As an applicable electronic device, a AlGa_N/Ga_N-based high electron mobility transistor (HEMT) is widely being examined to be realized by using a group III nitride semiconductor having a high electron transporting property.

10 [0005]

Now, a conventional AlGa_N/Ga_N-based HEMT will be described with reference to drawings.

[0006]

FIGS. **23A** and **23B** show the conventional AlGa_N/Ga_N-based HEMT, wherein FIG. **23A** shows the plane structure thereof and FIG. **23B** shows the cross-sectional structure thereof taken on line XXIIIB-XXIIIB of FIG. **23A**. As is shown in FIGS. **23A** and **23B**, a first HEMT **100A** and a second HEMT **100B** are formed on a substrate **101** of silicon carbide (SiC) so as to be separated by a scribe region **110**, used for dividing the substrate **101** into chips each including a transistor.

[0007]

Each of the first HEMT **100A** and the second HEMT **100B** includes, on a buffer layer **102** of Ga_N grown on the substrate **101**, an active region **103** formed by mesa-etching a

heterojunction layer of AlGa_N/Ga_N.

[0008]

On each active region **103**, a gate electrode **104** in Schottky contact with the active region **103** and ohmic electrodes **105**, in ohmic contact with the active region **103**, disposed with space from side edges along the gate length direction of the gate electrode **104** are formed.

[0009]

A portion above and around each active region **103** including the gate electrode **104** and the ohmic electrodes **105** is entirely covered with an insulating film **106**, and pad electrodes **107** respectively electrically connected to the gate electrode **104** and the ohmic electrodes **105** are formed on each insulating film **106**. The insulating film **106** is covered with a surface passivation film **108** with the pad electrodes **107** exposed.

[0010]

The insulating film **106** covering the active region **103** is generally formed from silicon oxide or the like, so as to protect the surface of the active region **103** and ease formation of the gate electrode **104** by a lift off method.

[0011]

As is shown in FIG. **23A**, since it is necessary to provide the gate electrode **104** with an extended portion **104a** to be connected to the pad electrode **107**, the gate electrode

104 is formed not only on the active region **103** but also on the buffer layer **102** of GaN exposed by the mesa-etching.

[0012]

[Problem that the Invention is to Solve]

5 In the conventional AlGaIn/GaN-based HEMT, however, contact between the extended portion **104a** and the buffer layer **102** is contact between a metal and a semiconductor, namely, the so-called Schottky contact, and hence, there is a problem that a leakage current tends to occur due to damage
10 of the semiconductor surface caused in the mesa-etching. This leakage current largely affects a pinch-off characteristic of the transistor, resulting in degrading the transistor characteristic.

[0013]

15 Furthermore, since adhesion between the buffer layer **102** of GaN and the insulating film **106** of silicon oxide is insufficient, there is another problem that the insulating film **106** peels off in wire-bonding the pad electrodes **107** formed on the insulating film **106**.

20 [0014]

 Moreover, both the substrate **101** of SiC and the GaN-based semiconductor have high hardness, and hence, it is very difficult to conduct a scribe process for dividing the substrate into chips as compared with the case where Si and
25 GaAs are used. Therefore, the yield may be lowered due to

occurrence of a crack reaching the active region **103** in the scribe process or the reliability may be lowered due to peeling of the surface passivation film **108** or the insulating film **106** in the vicinity of the scribe region **110**.

5 [0015]

In a semiconductor laser diode having a laser structure formed by multi layers of group III nitride semiconductors, a substrate of sapphire is generally used. In the case where sapphire is used as the substrate, it is difficult to form a
10 cavity structure by cleavage because of a difference in the crystal axis between sapphire and the laser structure formed on the sapphire, and hence, the cavity structure is frequently formed by dry etching. When the cavity is formed by dry etching, however, a defect peculiar to the formed
15 cavity facet is caused so as to form a non-luminescent center. As a result, there arises a problem that the operation current (threshold current) may increase or the reliability may be lowered.

[0016]

20 The present invention was devised for overcoming the aforementioned conventional problems, and an object of the invention is forming an insulating film having high adhesion to a group III nitride semiconductor, a good electric characteristic or a good optical characteristic.

25 [0017]

[Means of Solving the Problem]

In order to achieve the object, a semiconductor device including a group III nitride semiconductor of this invention has an oxide film formed by directly oxidizing the group III
5 nitride semiconductor itself.

[0018]

Specifically, the first semiconductor device of this invention comprises an active region formed on a substrate from a group III nitride semiconductor; and an insulating
10 oxide film formed in a peripheral portion of the active region on the substrate by oxidizing the group III nitride semiconductor.

[0019]

According to the first semiconductor device of this
15 invention, the insulating oxide film is formed in the peripheral region of the active region on the substrate by oxidizing the group III nitride semiconductor. Therefore, the bonding strength between a group III nitride semiconductor and an oxide film formed from an oxide of the group III
20 nitride semiconductor is approximately three times as large as the bonding strength between, for example, a group III nitride semiconductor and a silicon oxide film. Accordingly, the adhesion between the insulating oxide film and the substrate or between the insulating oxide film and the active
25 region is high in the first semiconductor device, so as to

prevent the insulating oxide film and the like from peeling off. As a result, the yield and the reliability of the semiconductor device can be improved.

[0020]

5 In the first semiconductor device, it is preferable that an ohmic electrode is formed on the active region and a gate electrode formed to extend from the active region onto the insulating oxide film. In this manner, even when a portion of the gate electrode positioned on the insulating
10 oxide film is used as an extended portion of the gate electrode, the extended portion is not in Schottky contact with the insulating oxide film formed by oxidizing the group III nitride semiconductor. Therefore, a leakage current can be prevented from flowing in the extended portion, resulting
15 in improving the reliability of the device.

[0021]

 The second semiconductor devices of this invention plural in the number comprise a group III nitride semiconductor formed in a plurality of device formation
20 regions each surrounded with a scribe region on a substrate in a wafer state; and a protection oxide film formed in a peripheral portion of the scribe region on the substrate by oxidizing the group III nitride semiconductor.

[0022]

25 According to the second semiconductor devices, the

protection oxide film is formed in the peripheral portion of the scribe region on the substrate by oxidizing the group III nitride semiconductor and the bonding strength between the group III nitride semiconductor and the protection oxide film is larger than the bonding strength between the group III nitride semiconductor and a silicon oxide film or the like. Therefore, in dividing the plural semiconductor devices formed on one wafer into chips, an insulating film covering the device formation region can be prevented from peeling off and cracks can be prevented from occurring in the device formation region, resulting in improving the yield and the reliability of the devices.

[0023]

The third semiconductor device of this invention comprises an active region formed on a substrate from a group III nitride semiconductor; and a pad electrode formed on a substrate; and an insulating oxide film formed between the substrate and the pad electrode by oxidizing a group III nitride semiconductor.

[0024]

According to the third semiconductor device, the insulating oxide film is formed between the substrate and the pad electrode by oxidizing the group III nitride semiconductor and the bonding strength between the group III nitride semiconductor and the insulating oxide film is larger than

the bonding strength between the group III nitride semiconductor and a silicon oxide film or the like. Therefore, the pad electrode can be prevented from peeling off from the substrate in the third semiconductor device, resulting in
5 improving the yield and the reliability of the device.

[0025]

The fourth semiconductor device of this invention comprises a laser structure formed on a substrate and having a cavity including a plurality of group III nitride
10 semiconductors; and a protection oxide film formed on side faces of the laser structure including facets of the cavity by oxidizing the group III nitride semiconductors.

[0026]

In the fourth semiconductor device, the protection
15 oxide film is formed on the side faces of the laser structure including facets of the cavity by oxidizing the group III nitride semiconductors. Therefore, a mirror face of a cavity mirror is not an etched facet but is formed from an interface between the etched facet and the protection oxide film, and
20 hence, the mirror face is never affected by a defect caused in etching. In addition, the group III nitride semiconductor is directly oxidized, and hence, a leakage current derived from a defective facet coating can be avoided, resulting in attaining high reliability.

25 [0027]

The first method of fabricating a semiconductor device of this invention comprises a semiconductor layer forming step of forming a group III nitride semiconductor layer on a substrate; a protection film forming step of forming, on the group III nitride semiconductor layer, a protection film for covering an active region of the group III nitride semiconductor layer; an oxide film forming step of forming, in a region on the substrate excluding the active region, an insulating oxide film by oxidizing the group III nitride semiconductor layer with the protection film used as a mask; and an active region exposing step of exposing the active region by removing the protection film.

[0028]

In the first method of fabricating a semiconductor device, the protection film for covering the active region of the group III nitride semiconductor layer is formed, and then the insulating oxide film is formed in the region on the substrate excluding the active region by oxidizing the group III nitride semiconductor layer with the protection film used as a mask. Therefore, the first semiconductor device of this invention can be definitely fabricated.

[0029]

The first method of fabricating a semiconductor device of this invention preferably further comprises, after the active region exposing step, an ohmic electrode forming step

of forming an ohmic electrode on the active region; and a gate electrode forming step of forming, on the active region, a gate electrode extending onto the insulating oxide film.

[0030]

5 The first method of fabricating a semiconductor device of this invention preferably further comprises, between the semiconductor layer forming step and the protection film forming step, an ammonia treatment step of exposing the group III nitride semiconductor laser to ammonia. In this manner,
10 an oxide or the like remaining on the surface of a device formation region to be used as the active region is removed and cleaned by ammonia, and hence, the contact resistance ratio of the active region can be lowered. As a result, the electric characteristic of the device can be improved.

15 [0031]

In this case, the ammonia treatment step preferably includes a sub-step of changing the ammonia into plasma.

[0032]

20 The second method of fabricating a semiconductor device of this invention comprises a semiconductor layer forming step of forming a group III nitride semiconductor layer on a substrate in a wafer state; a region setting step of setting, in the group III nitride semiconductor layer, a plurality of device formation regions where devices are to be formed on
25 the group III nitride semiconductor layer and a scribe region

for used in dividing the substrate into chips respectively including the device formation regions; a protection film forming step of forming, on the scribe region, a protection film for covering the scribe region; and an oxide film forming step of forming, in a region on sides of the scribe region on the substrate, a protection oxide film by oxidizing the group III nitride semiconductor layer with the protection film used as a mask.

[0033]

10 In the second method of fabricating a semiconductor device, the protection film for covering the scribe region is formed, and then the protection oxide film is formed on sides of the scribe region on the substrate with the protection film used as a mask. Therefore, the second semiconductor
15 device of this invention in which the insulating film covering the device formation region can be prevented from peeling off and cracks can be prevented from occurring in the device formation region can be definitely fabricated.

[0034]

20 In the first or second method of fabricating a semiconductor device, the protection film is preferably formed from silicon, silicon oxide or silicon nitride.

[0035]

The third method of fabricating a semiconductor device
25 of this invention comprises a semiconductor layer forming

step of forming a group III nitride semiconductor layer on a substrate; a region setting step of setting, in the group III nitride semiconductor layer, a device formation region where a device is to be formed on the group III nitride semiconductor layer and a pad electrode formation region for external connection of the device to be formed in the device formation region; a protection film forming step of forming a protection film covering a region on the group III nitride semiconductor layer excluding the pad electrode formation region; an oxide film forming step of forming an insulating oxide film in the pad electrode formation region on the substrate by oxidizing the group III nitride semiconductor layer with the protection film used as a mask; and a step of forming a pad electrode on the insulating oxide film.

15 [0036]

In the third method of fabricating a semiconductor device, the protection film covering the region on the group III nitride semiconductor layer excluding the pad electrode formation region is formed, and then the insulating oxide film is formed in the pad electrode formation region on the substrate by oxidizing the group III nitride semiconductor layer with the protection film used as a mask. Accordingly, the third semiconductor device of the invention can be definitely fabricated.

25 [0037]

In any of the first through third methods of fabricating a semiconductor device, the oxide film forming step preferably includes a sub-step of conducting a thermal treatment on the group III nitride semiconductor layer in an oxygen ambient.

[0038]

In any of the first through third methods of fabricating a semiconductor device, the oxide film forming step preferably includes a sub-step of conducting a thermal treatment on the group III nitride semiconductor layer with oxygen ions implanted.

[0039]

The fourth method of fabricating a semiconductor device of this invention comprises a laser structure forming step of forming, on a substrate, a laser structure having a cavity and including a plurality of group III nitride semiconductor layers by forming the plurality of group III nitride semiconductor layers; a step of exposing facets of the cavity of the laser structure; and an oxide film forming step of forming a protection oxide film on the facets by oxidizing side faces of the laser structure including the facets.

[0040]

In the fourth method of fabricating a semiconductor device, the facets of the cavity of the laser structure are exposed, and then the protection oxide film is formed on both

side faces of the laser structure including the facets of the cavity by oxidizing the group III nitride semiconductor layers. Therefore, the fourth semiconductor device of the invention can be definitely fabricated. Also, since a procedure for forming facet coating can be omitted, the fabrication can be simplified.

[0041]

In the fourth method of fabricating a semiconductor device, the oxide film forming step preferably includes a sub-step of conducting a thermal treatment on the group III nitride semiconductor layers in an oxygen ambient.

[0042]

[Mode for Carrying Out the Invention]

(EMBODIMENT 1)

Embodiment 1 of the invention will now be described with reference to the accompanying drawings.

[0043]

FIGS. **1A** and **1B** show an HEMT including a group III nitride semiconductor, particularly, an oxide-isolated HEMT in which devices are isolated by a GaN-based oxide, according to Embodiment 1 of the invention, wherein FIG. **1A** is a plane view thereof and FIG. **1B** is a cross-sectional view thereof taken on line IB-IB of FIG. **1A**. As is shown in FIGS. **1A** and **1B**, the HEMT of this embodiment includes an active region **12A** of a GaN-based semiconductor grown on a substrate **11** of, for

example, silicon carbide (SiC) and an insulating oxide film **12B** formed around the active region **12A** by oxidizing the GaN-based semiconductor.

[0044]

5 On the active region **12A**, a gate electrode **13** in Schottky contact with the active region **12A** is formed so as to extend onto the insulating oxide film **12B** and have an extended portion **13a** on the insulating oxide film **12B**, and ohmic electrodes **14** respectively serving as a source
10 electrode and a drain electrode are formed with space from the side edges along the gate length direction of the gate electrode **13**.

[0045]

Now, a conventional mesa-isolated HEMT and the oxide-
15 isolated HEMT of this embodiment will be compared in the voltage-current characteristic between the Schottky electrode and the ohmic electrode. FIG. **24** shows the cross-sectional structure of a pseudo device simulating the conventional mesa-isolated HEMT. Specifically, on a substrate **121** of SiC,
20 an island-like active layer **122** of a GaN-based semiconductor, an island-like ohmic electrode **123** formed on the active layer **122** and a Schottky electrode **124** in Schottky contact with the substrate with a space from the active layer **122** are formed. In this case, the Schottky electrode **124** corresponds to the
25 extended portion **104a** shown in FIG. **23A**. The pseudo device

exhibits a rectified current characteristic as is shown in FIG. 25, and although the reverse breakdown voltage is large, a leakage current flows on the order of microampere (μ A). In this manner, in the conventional mesa-isolated HEMT shown in
5 FIGS. 23A and 23B, the extended portion 104a of the gate electrode 104 is formed on the buffer layer 102 of mesa-etched GaN. Therefore, the contact between the extended portion 104a of the gate electrode 104 and the buffer layer 102 is Schottky contact, so that a leakage current can easily
10 flow.

[0046]

On the other hand, in the oxide-isolated HEMT of this embodiment, the voltage-current characteristic between the Schottky electrode 13 formed on the insulating oxide film 12B
15 and the ohmic electrode 14 formed on the active region 12A is shown in FIG. 2. Thus, even when a voltage of 100 V or more is applied between these electrodes, merely a current on the order of nanoampere (nA) flows.

[0047]

20 FIG. 3 shows the gate voltage dependency of a drain current in the oxide-isolated HEMT of this embodiment and the conventional mesa-isolated HEMT both having a gate width of 100 μ m. Although there is no particular difference in a region where the gate voltage is so high that a large drain
25 current flows, there is a large difference in the vicinity of

pinch-off where a small drain current flows. It is thus understood that the pinch-off characteristic is degraded in the conventional mesa-isolated HEMT owing to a leakage current caused in the extended portion **104a** of the gate electrode **104**.

[0048]

In this manner, in the oxide-isolated HEMT of this embodiment, a leakage current can be avoided from flowing in the extended portion **13a** of the gate electrode differently from the conventional mesa-isolated HEMT, so that the HEMT can attain a good pinch-off characteristic.

[0049]

Furthermore, in the oxide-isolated HEMT of this embodiment, the insulating oxide film **12B** is formed by oxidizing the group III nitride semiconductor (GaN) used for forming the active region **12A**, and therefore, a level difference like that of the mesa-isolated HEMT is never caused in the boundary between the side edge portion of the active region **12A** and the insulating oxide film **12B** but the boundary is smooth. In the gate electrode **104** of the conventional HEMT, there is a fear of the so-called level disconnection that the gate electrode **104** is disconnected due to a level difference between the side edge of the active region **103** and the top face of the buffer layer **102** during, for example, the fabrication. On the contrary, there is no

fear of the level disconnection in this embodiment owing to the smooth boundary, resulting in attaining high reliability.

[0050]

Although the HEMT is described in this embodiment, the same effects can be attained in any device requiring isolation, such as a field effect transistor (MESFET) and a hetero bipolar transistor (HBT).

[0051]

Although the substrate of silicon carbide (SiC) is used in the HEMT of this embodiment, any substrate on which an active region of a group III nitride semiconductor can be epitaxially grown, such as a sapphire substrate, may be used instead.

[0052]

Now, a method of fabricating the oxide-isolated HEMT having the aforementioned structure will be described with reference to the accompanying drawings.

[0053]

FIGS. **4A** through **4C** and **5A** through **5C** are cross-sectional views for showing procedures in the method of fabricating the oxide-isolated HEMT of this embodiment.

[0054]

First, as is shown in FIG. **4A**, a multi-layer structure **12** of GaN/AlGaN is formed on a substrate **11** of SiC by, for example, electron beam epitaxy (MBE). The detailed structure

of the multi-layer structure **12** will be described later.

[0055]

Next, as is shown in FIG. **4B**, a protection formation film of silicon (Si) is formed on the entire surface of the multi-layer structure **12** by, for example, chemical vapor deposition (CVD) or the MBE. Thereafter, the protection formation film is patterned by lithography into a protection film **21** covering an island-like active formation region **20** on the multi-layer structure **12**.

10 [0056]

Then, as is shown in FIG. **4C**, with the protection film **21** formed on the multi-layer structure **12**, a thermal treatment is carried out at approximately 900°C in an oxygen ambient for approximately 1 hour. Thus, a portion of the multi-layer structure **12** excluding an active region **12A** is oxidized into an insulating oxide film **12B**.

[0057]

Subsequently, as is shown in FIG. **5A**, the protection film **21** is removed by using nitric acid/hydrogen fluoride, so as to expose the active region **12A**. Thereafter, as is shown in FIG. **5B**, ohmic electrodes **14** of titanium (Ti)/aluminum (Al) are selectively formed on the active region **12A** by deposition and lithography.

[0058]

25 Next, as is shown in FIG. **5C**, a gate electrode **13** of,

for example, palladium (Pd)/titanium (Ti)/gold (Au) is selectively formed on the active region **12A** by the deposition and the lithography, so as to be sandwiched by the ohmic electrodes **14** with space therebetween and to extend onto the
5 insulating oxide film **12B**. Thereafter, although not shown in the drawings, a protection insulating film of, for example, a silicon oxide film is formed above and around the active region **12A** including the gate electrode **13** and the ohmic electrodes **14**. Then, pad electrodes of, for example, titanium
10 (Ti)/gold (Au) respectively electrically connected to the gate electrode **13** and the ohmic electrodes **14** are formed on the protection insulating film.

[0059]

In this manner, in the HEMT of this embodiment,
15 isolation is provided by directly oxidizing the group III nitride semiconductor used for forming the active region **12A**. Next, the isolation characteristic between the active region **12A** and the insulating oxide film **12B** formed as described above and the substrate characteristic of the active region
20 **12A**, which are extremely significant for the operation characteristic of the HEMT, will be verified.

[0060]

FIG. 6 is a cross-sectional view of a multi-layer structure **12** used for the verification. The multi-layer
25 structure **12** includes the following layers successively grown

on a substrate **11**: A buffer layer **31** of aluminum nitride (AlN) with a thickness of approximately 100 nm; an active layer **32** of intrinsic gallium nitride (GaN) with a thickness of approximately 3 μm ; a first barrier layer **33** of intrinsic aluminum gallium nitride (AlGaN) with a thickness of approximately 2 nm; a second barrier layer **34** of n-type aluminum gallium nitride (AlGaN) with a thickness of approximately 25 nm; and a third barrier layer **35** of intrinsic aluminum gallium nitride (AlGaN) with a thickness of approximately 3 nm.

[0061]

FIG. 7 shows the dependency on thermal treatment time of the thickness of the insulating oxide film **12B** formed by subjecting the multi-layer structure **12** to a thermal treatment conducted at 900°C in an oxygen ambient. As is shown in FIG. 7, the thermal treatment carried out for 1 hour results in forming an insulating oxide film with a thickness of approximately 100 nm, and the thermal treatment carried out for 4 hours results in forming an insulating oxide film with a thickness of approximately 200 nm. Since the total thickness of the barrier layers **33** through **35** of the HEMT is approximately 30 nm as is shown in FIG. 6, the insulating oxide film **12B** with a thickness of approximately 100 nm suffices.

[0062]

FIG. 8 shows the relationship between the thickness of the insulating oxide film **12B** and a leakage current flowing between devices isolated by the insulating oxide film. It is understood from FIG. 8 that a satisfactory isolation characteristic can be attained when the insulating oxide film **12B** has a thickness of 80 nm or more. Accordingly, as is obvious from FIGS. 7 and 8, when the thermal treatment is carried out at 900°C, the devices can be sufficiently isolated by conducting the thermal treatment approximately for 1 hour.

[0063]

In forming the insulating oxide film **12B**, the thermal treatment may be carried out, instead of in an oxygen ambient, with oxygen ions implanted into the multi-layer structure **12**.

[0064]

Next, the substrate characteristic will be verified.

[0065]

The substrate characteristic of the active region **12A** should never degrade through the thermal treatment. Therefore, in order to avoid oxidation of the active region **12A** through the thermal treatment, the protection film **21** is formed from silicon (Si) in this embodiment.

[0066]

FIGS. **9A** through **9C** show atomic profiles along a depth direction of the substrate of the HEMT of this embodiment

obtained by Auger electron spectroscopy (AES) analysis. FIG. **9A** shows the profile of the isolation (insulating oxide film **12B**) obtained after conducting a thermal treatment at 900°C for 1 hour and removing the protection film **21**, FIG. **9B** shows the profile of the active region **12A** masked with the protection film **21** with a thickness of approximately 100 nm and FIG. **9C** shows, for comparison, the profile of the multi-layer structure **12** not subjected to the thermal treatment. In these graphs, "Ga" indicates the profile of gallium atoms, "N" indicates the profile of nitrogen atoms and "O" indicates the profile of oxygen atoms. Also, since attention is paid to the profile of oxygen atoms in the multi-layer structure **12**, aluminum atoms in a trace quantity are omitted. In these graphs, the abscissa indicates the depth (nm) from the surface of a sample and the ordinate indicates a relative value (peak-to-peak).

[0067]

As is shown in FIG. **9A**, the structure of the multi-layer structure **12** prior to the thermal treatment is largely broken in the isolation, so that the oxygen atoms are diffused from the top face to the active layer **32**, resulting in forming the insulating oxide film **12B**. In this case, the insulating oxide film **12B** has a thickness of approximately 100 nm.

[0068]

Furthermore, as is shown in FIG. **9B**, in the active region **12A** masked with the protection film **21** of Si, although the upper portion of the protection film **21** is oxidized, there is no reaction on the interface between the protection
5 film **21** and the active region **12A**. Thus, the structure of the active region **12A** prior to the thermal treatment is not changed but kept as is understood from comparison with the profile of FIG. **9C** obtained without the thermal treatment.

[0069]

10 Furthermore, Table 1 below shows the sheet carrier concentration and the carrier mobility of the multi-layer structure **12** obtained before and after the thermal treatment by a Hall measurement method at room temperature.

[0070]

15 [Table 1]

	Before thermal treatment	After thermal treatment
Carrier concentration (cm ⁻³)	1.4 x 10 ¹³	1.5 x 10 ¹³
Mobility (cm ² /Vs)	741	766

[0071]

Neither of the sheet carrier concentration and the carrier mobility is largely changed before and after the
20 thermal treatment. It is understood also from this result that the active region **12A** is protected by the protection film **21** as is understood from the result of the AES analysis.

[0072]

Furthermore, the removing process of the protection film **21** after the thermal treatment is also significant in this invention. If the protection film **21** cannot be completely removed or the active region **12A** is damaged in removing the protection film **21**, the transistor characteristic is degraded. In addition, the insulating oxide film **12B** should never be etched in removing the protection film **21**.

10 [0073]

Accordingly, the protection film **21** of Si is removed in this embodiment by wet etching using nitric acid/hydrogen fluoride.

[0074]

15 FIG. **10** shows time dependency of the etching amount in the wet etching using nitric acid/hydrogen fluoride of the protection film **21** and the insulating oxide film **12B** after the thermal treatment. As is shown in FIG. **10**, although the protection film **21** is easily etched, the insulating oxide film **12B** is minimally etched.

20 [0075]

Although the protection film **21** is removed by the wet etching using nitric acid/hydrogen fluoride in this embodiment, another etchant may be used instead. Alternatively, the etching may be carried out by dry etching.

[0076]

Furthermore, although the protection film **21** is formed from silicon in this embodiment, any other material capable of preventing degradation of the active region **12A** through the thermal treatment, such as silicon oxide and silicon nitride, may be used instead. A solution including fluoric acid such as buffered hydrogen fluoride (BHF) may be used as the etchant when the protection film is formed from silicon oxide, and a solution including phosphoric acid such as heated phosphoric acid may be used as the etchant when the protection film is formed from silicon nitride.

[0077]

(MODIFICATION OF EMBODIMENT 1)

A method of fabricating a semiconductor device according to one modification of Embodiment 1 will now be described with reference to the accompanying drawing. The fabrication method of this modification is characterized by including an ammonia treatment process for exposing the top face of the multi-layer structure **12** to plasma of an ammonia gas between the process for forming the multi-layer structure shown in FIG. **4A** and the process for forming the protection film shown in FIG. **4B**.

[0078]

FIG. **11** shows the result of evaluation of contact resistance of an ohmic electrode **14** formed on an active

region **12A** obtained by a transmission line method (TLM). In this evaluation, the ohmic electrode **14** has a width of approximately 100 μm , and the spacing between the ohmic electrodes **14** is set to 2 μm , 4 μm , 6 μm or 8 μm . The result
5 obtained with the ammonia treatment of this modification carried out is shown with a solid line, and the result obtained without the ammonia treatment is shown with a broken line for comparison. As is shown in FIG. **11**, the inclination of the line obtained with the ammonia treatment is
10 substantially the same as that of the line obtained without the ammonia treatment, which reveals that there is no difference in the sheet resistance of the active region **12A** between these cases. On the contrary, the contact resistance is lowered by approximately 30% when the ammonia treatment is
15 carried out as compared with when it is not carried out. The contact resistance ratio obtained based on this graph is $6 \times 10^{-6} \Omega \text{ cm}^2$, which is a satisfactory value, even when the ammonia treatment is not carried out, and is as low as $3 \times 10^{-6} \Omega \text{ cm}^2$ when the ammonia treatment is carried out. This is
20 because altered substances such as an oxide present on the active region **12A** are removed and cleaned by the ammonia treatment.

[0079]

Although the ammonia treatment is carried out by using
25 plasma of an ammonia gas in this modification, the ammonia

treatment may be carried out by boiling the multi-layer structure in an ammonia solution.

[0080]

(EMBODIMENT 2)

5 Embodiment 2 of the invention will now be described with reference to the accompanying drawings.

[0081]

FIG. 12 shows the cross-sectional structure of a scribe region of a GaN-based semiconductor device of Embodiment 2.

10 The GaN-based semiconductor device of this embodiment is characterized by including a protection oxide film formed by oxidizing a GaN-based semiconductor itself in the periphery of a scribe region used in scribing a wafer bearing a plurality of semiconductor devices into chips including the

15 respective semiconductor devices. As is shown in FIG. 12, the principal plane of a substrate **42** of, for example, SiC in a wafer state is partitioned into chip formation regions **40** and a scribe region **41** provided between the chip formation regions **40**.

20 [0082]

In the scribe region **41** on the principal plane of the substrate **42**, a multi-layer structure **43A** of GaN-based semiconductors to be used as an active layer for a transistor or the like in a device formation region (not shown) formed

25 at the center of the chip formation region **40** is formed. In a

peripheral portion of the scribe region **41** on the principal plane in the vicinity of the chip formation region **40**, a protection oxide film **43B** formed by oxidizing the multi-layer structure **43A** is formed and an insulating film **44** of a silicon oxide film or the like serving as a surface protection film is formed on the protection oxide film **43B**.

[0083]

In a conventional GaN-based semiconductor device, a peripheral portion of a scribe region **41** is covered with an insulating film **44** of a silicon oxide film or the like having comparatively small bonding strength with a GaN-based semiconductor, and hence, the insulating film **44** is easily peeled off during scribing (division into chips). The insulating film **44** of this embodiment is formed on the protection insulating film **43B** formed by oxidizing the GaN-based semiconductor having comparatively high bonding strength with the insulating film **44**, and hence, occurrence of cracks in the multi-layer structure **43A** and the substrate **42** and peeling of the insulating film **44** can be avoided in dividing the substrate **42** into chips.

[0084]

FIG. **13** shows the relationship, in the semiconductor device in a wafer state of this embodiment and a conventional semiconductor device in a wafer state, between the defective ratio in scribing and the width of the scribe region. Through

observation of the surface of each chip obtained when the scribe region has a width of 100 μm , it is found, in the conventional semiconductor chips, that defects are caused in approximately 20% of samples, specifically, a crack caused in
5 a multi-layer structure in the scribe region reaches the peripheral portion or inside of the chip, and the insulating film on the device formation region is peeled off.

[0085]

In contrast, through observation of the surface of the
10 chips of the semiconductor devices of this embodiment, it is found that a crack caused in the multi-layer structure **43A** in the scribe region **41** stops around the boundary with the protection oxide film **43B** so as not to reach the chip formation region **40**.

15 [0086]

As is understood from FIG. **13**, since the protection oxide film **43A** formed by oxidizing the GaN-based semiconductor is formed in the peripheral portion of the scribe region **41**, even when the scribe region **41** has a width
20 as small as approximately 100 μm , the defective ratio is lower than that in a conventional semiconductor device having a scribe region with a width of 150 μm . As a result, since the defective ratio in scribing can be suppressed in the semiconductor devices of this embodiment even when the width
25 of the scribe region **41** is small, the number of semiconductor

devices obtained from one substrate **42** (wafer) can be increased. In addition, the insulating film **44** can be prevented from peeling off, resulting in largely improving the reliability of the devices.

5 [0087]

Although the protection oxide film **43B** is formed also in the chip formation region **40** in this embodiment, a protection oxide film **43C** may be formed instead in a circular shape along the edge of the scribe region **41** as a
10 modification as is shown in FIG. **14**. In this case, the protection oxide film **43C** with a width of approximately 5 μm suffices.

[0088]

Although the substrate **42** is formed from SiC in this
15 embodiment, any substrate on which the multi-layer structure **43A** of GaN-based semiconductors can be epitaxially grown, such as a sapphire substrate, may be used instead.

[0089]

Now, a method of fabricating the semiconductor device
20 having the aforementioned structure will be described with reference to the accompanying drawings.

[0090]

FIGS. **15A** through **15C**, **16A** and **16B** are cross-sectional views for showing procedures in the method of fabricating the
25 semiconductor device of this embodiment.

[0091]

First, as is shown in FIG. **15A**, a multi-layer structure **43A** of GaN/AlGaN is formed on a wafer-like substrate **42** of SiC by, for example, the electron beam epitaxy (MBE).

5 [0092]

Next, as is shown in FIG. **15B**, plural chip formation regions **40** and a scribe region **41** between the plural chip formation regions **40** are formed. In the scribe region **41**, a protection formation film of Si is formed on the multi-layer structure **43A** by the CVD or the like, and the protection formation film is patterned by the lithography into a protection film **21** covering the scribe region **41** on the substrate **42**.

[0093]

15 Then, as is shown in FIG. **15C**, with the protection film **21** formed on the multi-layer structure **43A**, a thermal treatment is carried out at approximately 900°C in an oxygen ambient for approximately 1 hour. Thus, portions of the multi-layer structure **43A** positioned in the chip formation regions **40** on both sides of the scribe region **41** are oxidized into protection oxide films **43B**.

[0094]

The protection oxide film **43B** may be formed before or after forming a semiconductor device such as a transistor in a device formation region (not shown) at the center of the

25

chip formation region **40**, whereas it is preferably formed before forming the semiconductor device for attaining a good device characteristic because the thermal treatment is carried out at a comparatively high temperature. In this case, the protection oxide film **43B** may be formed in the same procedure for forming the protection film **21** shown in FIG. **4C** described in Embodiment 1.

[0095]

Subsequently, as is shown in FIG. **16A**, the protection film **21** is removed by using nitric acid/hydrogen fluoride, and then, as is shown in FIG. **16B**, an insulating film **44** of, for example, silicon oxide for surface protection is formed on the entire surface of the chip formation regions **40** by the CVD or the like. Then, the insulating film **44** is selectively etched by the lithography so as to expose the multi-layer structure **43A** in the scribe region **41**.

[0096]

In this manner, since the protection oxide film **43B** is formed from an oxide of the multi-layer structure **43A** of GaN-based semiconductors in this embodiment, the adhesion between the substrate **42** and the insulating film **44** is high. Also, since the multi-layer structure **43A** and the protection oxide film **43B** are continuously formed in the scribe region **41**, even when a crack is caused in the protection oxide film **43B** in scribing the substrate **42**, the crack can be prevented from

reaching the peripheral portion or inside of the chip formation region **40**.

[0097]

Although the protection film **21** used in masking the portion of the multi-layer structure **43A** in the scribe region **41** for forming the protection oxide film **43B** is formed from silicon in this embodiment, the protection film **21** may be formed from any material capable of preventing degradation of the multi-layer structure **43A** through the thermal treatment, such as silicon oxide and silicon nitride.

[0098]

Although the protection film **21** is removed by the wet etching using nitric acid/hydrogen fluoride, another etchant may be used. Alternatively, the etching can be carried out by dry etching.

[0099]

Furthermore, the thermal oxidation process for forming the protection oxide film **43B** may be carried out, instead of in an oxygen ambient, by implanting oxygen ions into the multi-layer structure **43A** of the GaN-based semiconductors.

[0100]

(EMBODIMENT 3)

Embodiment 3 of the invention will now be described with reference to the accompanying drawings.

[0101]

FIG. 17 shows the cross-sectional structure of a pad electrode portion serving as an external input/output terminal of a GaN-based semiconductor device of Embodiment 3. As is shown in FIG. 17, the principal plane of a wafer-like substrate 52 of, for example, SiC is partitioned into device formation regions 50 and a pad electrode formation region 51 adjacent to the device formation region 50.

[0102]

In the device formation region 50 on the principal plane of the substrate 52, a multi-layer structure 53A of GaN-based semiconductors serving as an active layer of a transistor or the like is formed, and in the pad electrode formation region 51, an insulating oxide film 53B formed by oxidizing the multi-layer structure 53A and a pad electrode 54 of, for example, titanium (Ti)/gold (Au) disposed on the insulating oxide film 53B are formed. Although not shown in the drawing, it goes without saying that the pad electrode 54 is electrically connected to a device (not shown) formed in the device formation region 50 through a wire.

[0103]

In this manner, the pad electrode 54 of this embodiment is formed above the multi-layer structure 53A of GaN-based semiconductors with the insulating oxide film 53B formed by oxidizing the multi-layer structure 53A sandwiched therebetween, and hence, adhesion between the pad electrode

54 and the substrate 52 can be improved. Accordingly, for example, the pad electrode 54 can be prevented from peeling off from the substrate 52 in wire-bonding the pad electrode 54.

5 [0104]

Table 2 below shows results of quantitatively evaluating adhesion of a GaN layer epitaxially grown on a substrate of SiC to a variety of thin film materials and adhesion of an oxide film formed by oxidizing an upper
10 portion of the GaN layer to a variety of thin film materials. This evaluation is made by a Sebastian method.

[0105]

[Table 2]

Sample structures	Tensile load (x 9.8 N/cm ²)
Silicon oxide film on GaN layer	350
Silicon nitride film on GaN layer	320
GaN oxide layer on GaN	1080
Ti/Au multi-layer structure on GaN oxide layer	850
Al on GaN oxide layer	830
Silicon oxide film on GaN oxide layer	920
Silicon nitride film on GaN oxide layer	900

15 [0106]

It is understood from Table 2 that an insulating film having high adhesion on a GaN layer is merely a GaN oxide layer formed by oxidizing a GaN layer. Furthermore, it is understood that a GaN oxide layer has high adhesion to not
20 only a metal material but also an insulating film including

silicon. Accordingly, a pad electrode portion required to have high adhesion is very effectively formed on the insulating oxide film **53B** obtained by oxidizing the multi-layer structure **53A** of GaN-based semiconductors.

5 [0107]

Although the substrate **52** is made from SiC in this embodiment, any substrate on which the multi-layer structure **53A** of GaN-based semiconductors can be epitaxially grown, such as a sapphire substrate, may be used instead.

10 [0108]

Now, a method of fabricating the pad electrode portion of a semiconductor device having the aforementioned structure will be described with reference to the accompanying drawings.

[0109]

15 FIGS. **18A** through **18C**, **19A** and **19B** are cross-sectional views for showing procedures in the method of fabricating the pad electrode portion of a semiconductor device of this embodiment.

[0110]

20 First, as is shown in FIG. **18A**, a multi-layer structure **53A** of GaN/AlGaN is formed on a substrate **52** of SiC by, for example, the electron beam epitaxy (MBE).

[0111]

Next, as is shown in FIG. **18B**, the entire surface of
25 the multi-layer structure **53A** is partitioned into device

formation regions **50** and pad electrode formation regions **51**. Subsequently, in the device formation region **50**, a protection formation film of Si is formed on the multi-layer structure **53A** by the CVD or the like. Thereafter, the protection formation film is patterned by the lithography into a protection film **21** covering the device formation region **50** on the substrate **52**.

[0112]

Then, as is shown in FIG. **18C**, with the protection film **21** formed on the multi-layer structure **53A**, a thermal treatment is carried out at approximately 900°C in an oxygen ambient for approximately 1 hour, thereby oxidizing a portion of the multi-layer structure **53A** in the pad electrode formation region **51** into an insulating oxide film **53B**.

[0113]

The insulating oxide film **53B** may be formed before or after forming a semiconductor device such as a transistor in the device formation region **50**, whereas it is preferably formed before forming the device for attaining a good device characteristic because the thermal treatment is carried out at a comparatively high temperature. In this case, the insulating oxide film **53B** is formed in the same procedure for forming the protection film **21** shown in FIG. **4C** of Embodiment 1 or shown in FIG. **15C** of Embodiment 2.

[0114]

Subsequently, as is shown in FIG. **19A**, the protection film **21** is removed by using nitric acid/hydrogen fluoride, and then, as is shown in FIG. **19B**, a pad electrode **54** of Ti/Au is selectively formed on the insulating oxide film **53B** in the pad electrode formation region **51** by, for example, the deposition and the lithography.

[0115]

In this manner, the pad electrode **54** is formed on the insulating oxide film **53B** obtained by oxidizing the multi-layer structure **53A** of GaN-based semiconductors in this embodiment, and hence, high adhesion can be attained.

[0116]

Although the pad electrode **54** is directly formed on the insulating oxide film **53B** in this embodiment, an insulating film such as a silicon oxide film and a silicon nitride film may be disposed between the pad electrode **54** and the insulating oxide film **53B** of an oxide of the GaN-based semiconductors because an insulating film including silicon has high adhesion to the oxide of the GaN-based semiconductors as is shown in Table 2.

[0117]

Although the protection film **21** for protecting a portion of the multi-layer structure **53A** in the device formation region **50** is made from silicon in this embodiment, any material capable of preventing degradation of the multi-

layer structure **53A** through the thermal treatment, such as a silicon oxide film and a silicon nitride film, may be used instead.

[0118]

5 Although the protection film **21** is removed by the wet etching using nitric acid/hydrogen fluoride in this embodiment, another etchant may be used. Alternatively, the etching can be carried out by dry etching.

[0119]

10 Furthermore, the insulating oxide film **53B** may be formed, instead of in an oxygen ambient, by implanting oxygen ions into the multi-layer structure **53A**.

[0120]

(EMBODIMENT 4)

15 Embodiment 4 of the invention will now be described with reference to the accompanying drawings.

[0121]

FIGS. **20A** and **20B** show a group III nitride semiconductor laser diode according to Embodiment 4 of the invention, wherein FIG. **20A** is a perspective view thereof and FIG. **20B** is a cross-sectional view thereof taken on line XXB-XXB of FIG. **20A**. As is shown in FIG. **20A**, the semiconductor laser diode of this embodiment includes the following layers successively formed on a substrate **61** of sapphire having the principal plane of the (0001) surface orientation: An n-type

20

25

contact layer **62** of n-type gallium nitride (GaN); an n-type cladding layer **63** of n-type aluminum gallium nitride (AlGaN); an active layer **64** of gallium indium nitride (GaInN); a p-type cladding layer **65** of p-type aluminum gallium nitride (AlGaN); and a p-type contact layer **66**. In this manner, the semiconductor laser diode has a laser structure **60A** including a cavity of doublehetero junction in which the active layer **64** including In is vertically sandwiched between the n-type cladding layer **63** and the p-type cladding layer **65** including Al. In this case, as is shown in FIGS. **20A** and **20B**, a direction in which an emitting facet **60a** opposes a reflecting facet **60b** of the laser structure **60A** corresponds to a lasing direction of a laser beam in the cavity.

[0122]

Also, as is shown in FIG. **20A**, on the p-type contact layer **66**, a p-side electrode **67** of, for example, nickel (Ni)/gold (Au) is formed. On the other hand, a part of the n-type contact layer **62** is exposed, so that an n-side electrode **68** of, for example, titanium (Ti)/aluminum (Al) can be formed on the exposed surface.

[0123]

As a characteristic of the semiconductor laser diode of this embodiment, as is shown in the cross-sectional view of FIG. **20B** along the emitting direction of a laser beam, the emitting facet **60a** and the reflecting facet **60b** working as

cavity mirrors in the laser structure **60A** are formed by etching the n-type cladding layer **63**, the active layer **64** and the p-type cladding layer **65** in a direction vertical to the principal plane of the substrate **61**, and the etched facets
5 are covered with a protection oxide film **70** formed by oxidizing the facets. Accordingly, a substantial cavity facet corresponds to the interface between the end of the active layer **64** and the protection oxide film **70**.

[0124]

10 Since the cavity mirror does not remain as the etched facet but is covered with the protection oxide film **70** in this manner, the semiconductor laser diode of this embodiment is minimally affected by defects or the like caused in the etching. Furthermore, the protection oxide film **70** is formed
15 by directly oxidizing the semiconductor layers included in the laser structure **60A**, and hence, no leakage current is caused, resulting in attaining high reliability.

[0125]

Moreover, since there is no need to provide a coating
20 on the cavity facet in the semiconductor laser diode of this embodiment, the number of fabrication processes can be reduced. It is necessary to optimize the reflectance of a laser beam on the emitting facet and the reflecting facet by adjusting the thickness of the protection oxide film **70** or
25 the like.

[0126]

Now, a method of fabricating the semiconductor laser diode having the aforementioned structure will be described with reference to the accompanying drawings.

5 [0127]

FIGS. **21A** through **21C** and **22A** through **22D** are cross-sectional views for showing procedures in the method of fabricating the semiconductor laser diode of this embodiment. In these drawings, the cross-sectional structure taken on
10 line XXB-XXB of FIG. **20A** is shown, whereas FIG. **21C** is a front view.

[0128]

First, as is shown in FIG. **21A**, an n-type contact layer **62**, an n-type cladding layer **63**, an active layer **64**, a p-type
15 cladding layer **65** and a p-type contact layer **66** are successively grown on a substrate **61** of sapphire by, for example, the metal organic vapor phase epitaxy (MOVPE).

[0129]

Next, as is shown in the cross-sectional view of FIG.
20 **21B** and the front view of FIG. **21C**, the p-type contact layer **66**, the p-type cladding layer **65**, the active layer **64** and the n-type cladding layer **63** are etched with a laser structure formation region **60** masked by, for example, electron cyclotron resonance (ECR) etching until the n-type contact
25 layer **62** is exposed. Thus, a laser structure **60A** including

the n-type contact layer **62**, the n-type cladding layer **63**, the active layer **64**, the p-type cladding layer **65** and the p-type contact layer **66** is formed, and an n-side electrode formation region **68A** is formed in the n-type contact layer **62**.

5 [0130]

Then, as is shown in the cross-sectional view of FIG. **22A**, a protection film **21** of silicon (Si) is selectively formed so as to cover a p-side electrode formation region **67A** and the n-side electrode formation region (not shown).

10 [0131]

Subsequently, as is shown in FIG. **22B**, with the protection film **21** formed on the laser structure **60A**, a thermal treatment is carried out at approximately 900°C in an oxygen ambient for approximately 1 hour, thereby forming a protection oxide film **70** on the top face and side faces excluding the p-side electrode formation region **67A** and the n-side electrode formation region of the laser structure **60A** by oxidizing corresponding portions of the laser structure **60A**.

20 [0132]

Next, as is shown in FIG. **22C**, the protection film **21** is removed by using nitric acid/hydrogen fluoride, thereby exposing the p-side electrode formation region **67A** on the p-type contact layer and the n-side electrode formation region.

25 [0133]

Then, as is shown in FIG. **22D**, a p-side electrode **67** is formed in the p-side electrode formation region **67A**, and an n-side electrode is formed in the n-side electrode formation region. In this manner, the semiconductor laser diode of FIG. **20A** is completed.

[0134]

In the fabrication method of this embodiment, since the GaN-based semiconductor layers included in the laser structure **60A** and their etched facets are oxidized, there is no need to provide coatings on the emitting facet **60a** and the reflecting facet **60b**, and the cavity mirrors can be formed on the interfaces between the protection oxide film **70** and the laser structure **60A**.

[0135] In the semiconductor laser diode of this embodiment, the active layer **64** may be formed into a striped shape or the p-type cladding layer **65** may be provided with a current confining layer in order to improve controllability in the lateral mode of the laser beam.

[0136]

Although the protection film **21** for masking the p-side electrode formation region **67A** and the n-side electrode formation region **68A** in forming the protection oxide film **70** is made from silicon in this embodiment, any material capable of preventing degradation of the p-type contact layer **66** and the n-type contact layer **62** through the thermal treatment,

such as a silicon oxide film and a silicon nitride film, may be used instead.

[0137]

Although the protection film **21** is removed by the wet
5 etching using nitric acid/hydrogen fluoride in this embodiment, another etchant may be used. Alternatively, the etching can be carried out by dry etching.

[0138]

Although the substrate **61** is made from sapphire in this
10 embodiment, any other substrate on which GaN-based semiconductor layers can be epitaxially grown, such as SiC, may be used instead of the sapphire substrate.

[0139]

[Effect of the Invention]

15 According to the first semiconductor device of the present invention and the method of fabricating the same of the present invention, an insulating oxide film is formed in a peripheral region of an active region on a substrate by oxidizing a group III nitride semiconductor. Therefore, the
20 adhesion between the insulating oxide film and the substrate or between the insulating oxide film and the active region is high. As a result, the yield and the reliability of the semiconductor device can be improved.

[0140]

25 According to the second semiconductor device of the

present invention and the method of fabricating the same of the present invention, a protection oxide film is formed in a peripheral portion of a scribe region on a substrate by oxidizing a group III nitride semiconductor. Therefore, 5 cracks can be prevented from occurring in the device formation region, resulting in improving the yield and the reliability of the devices.

[0141]

According to the third semiconductor device of the 10 present invention and the method of fabricating the same of the present invention, an insulating oxide film is formed between a substrate and a pad electrode by oxidizing a group II nitride semiconductor. Therefore, the pad electrode can be prevented from peeling off from the substrate, resulting in 15 improving the yield and the reliability of the device.

[0142]

According to the fourth semiconductor device of the present invention and the method of fabricating the same of the present invention, a protection oxide film is formed on 20 the side faces of a laser structure including facets of a cavity by oxidizing group III nitride semiconductors. Therefore, the device is never affected by a defect caused in etching, resulting in improving the reliability of the device.

[Brief Description of Drawings]

25 [FIG. 1] FIGS. 1A and 1B are diagrams of a GaN-based

oxide-isolated HEMT according to Embodiment 1 of the invention, wherein FIG. **1A** is a plane view thereof and FIG. **1B** is a cross-sectional view thereof taken on line IB-IB of FIG. **1A**.

5 [FIG. **2**]

FIG. **2** is a graph for showing a voltage-current characteristic between a Schottky electrode formed on an insulating oxide film and an ohmic electrode formed on an active region in the oxide-isolated HEMT of Embodiment 1.

10 [FIG. **3**]

FIG. **3** is a graph for showing gate voltage dependency of a drain current in the oxide-isolated HEMT of Embodiment 1 and a conventional mesa-isolated HEMT.

[FIG. **4**]

15 FIGS. **4A**, **4B** and **4C** are cross-sectional views for showing procedures in a method of fabricating the oxide-isolated HEMT of Embodiment 1.

[FIG. **5**]

20 FIGS. **5A**, **5B** and **5C** are cross-sectional views for showing other procedures in the method of fabricating the oxide-isolated HEMT of Embodiment 1.

[FIG. **6**]

25 FIG. **6** is a cross-sectional view of a multi-layer structure of GaN-based semiconductors in the oxide-isolated HEMT of Embodiment 1.

[FIG. 7]

FIG. 7 is a graph for showing dependency on thermal treatment time of the thickness of the insulating oxide film in the oxide-isolated HEMT of Embodiment 1.

5 [FIG. 8]

FIG. 8 is a graph for showing the relationship between the thickness of the insulating oxide film and a leakage current caused between elements in the oxide-isolated HEMT of Embodiment 1.

10 [FIG. 9]

FIGS. 9A, 9B and 9C show AES atomic profiles in a depth direction of a substrate of the oxide-isolated HEMT of Embodiment 1, wherein FIG. 9A is a graph of the insulating oxide film obtained after conducting a thermal treatment and removing a protection film, FIG. 9B is a graph of the active region masked with the protection film and FIG. 9C is a graph for comparison of the multi-layer structure not subjected to the thermal treatment.

[FIG. 10]

20 FIG. 10 is a graph for showing time dependency of the etching amount of wet etching using nitric acid/hydrogen fluoride in the protection film and the insulating oxide film conducted after the thermal treatment in the oxide-isolated HEMT of Embodiment 1.

25 [FIG. 11]

FIG. 11 is a graph for showing dependency on electrode spacing of contact resistance of the ohmic electrode with or without an ammonia treatment in the oxide-isolated HEMT of Embodiment 1.

5 [FIG. 12]

FIG. 12 is a cross-sectional view of a scribe region of a GaN-based semiconductor device in a wafer state according to Embodiment 2 of the invention.

[FIG. 13]

10 FIG. 13 is a graph for showing the relationship between a defective ratio in a scribe process and the width of the scribe region in the semiconductor device in a wafer state of Embodiment 2 and a conventional semiconductor device in a wafer state.

15 [FIG. 14]

FIG. 14 is a cross-sectional view of a scribe region of a GaN-based semiconductor device in a wafer state according to a modification of Embodiment 2.

[FIG. 15]

20 FIGS. 15A, 15B and 15C are cross-sectional views for showing procedures in a method of fabricating the semiconductor device of Embodiment 2.

[FIG. 16]

FIGS. 16A and 16B are cross-sectional views for showing
25 other procedures in the method of fabricating the

semiconductor device of Embodiment 2.

[FIG. 17]

FIG. 17 is a cross-sectional view of a pad electrode portion of a GaN-based semiconductor device according to Embodiment 3 of the invention.

[FIG. 18]

FIGS. 18A, 18B and 18C are cross-sectional views for showing procedures in a method of fabricating the semiconductor device of Embodiment 3.

10 [FIG. 19]

FIGS. 19A and 19B are cross-sectional views for showing other procedures in the method of fabricating the semiconductor device of Embodiment 3.

[FIG. 20]

15 FIGS. 20A and 20B are diagrams of a group III nitride semiconductor laser diode according to Embodiment 4 of the invention, wherein FIG. 20A is a perspective view thereof and FIG. 20B is a cross-sectional view thereof taken on line XXB-XXB of FIG. 20A.

20 [FIG. 21]

FIGS. 21A, 21B and 21C are diagrams for showing a method of fabricating the semiconductor laser diode of Embodiment 4, wherein FIG. 21A is a cross-sectional view attained after epitaxial growth, FIG. 21B is a cross-sectional view taken on line XXIB-XXIB of FIG. 21C and FIG.

21C is a front view of a laser structure.

[FIG. **22**]

FIGS. **22A**, **22B**, **22C** and **22D** are cross-sectional views for showing other procedures in the method of fabricating the semiconductor laser diode of Embodiment 4.

[FIG. **23**]

FIGS. **23A** and **23B** are diagrams of a conventional GaN-based semiconductor device in a wafer state, wherein FIG. **23A** is a plane view thereof and FIG. **23B** is a cross-sectional view thereof taken on line XXIIIIB-XXIIIIB of FIG. **23A**.

[FIG. **24**]

FIG. **24** is a cross-sectional view of a pseudo device for simulating a conventional mesa-isolated HEMT.

[FIG. **25**]

FIG. **25** is a graph for showing a voltage-current characteristic between a Schottky electrode and an ohmic electrode formed on an active region of the pseudo device of FIG. **24**.

[Explanation of Reference Numerals]

- | | | |
|----|-----|-----------------------|
| 20 | 11 | Substrate |
| | 12 | Multi-layer structure |
| | 12A | Active region |
| | 12B | Insulating oxide film |
| | 13 | Gate electrode |
| 25 | 13a | Extended portion |

	14	Ohmic electrode
	20	Active formation region
	21	Protection film
	31	Buffer layer
5	32	Active layer
	33	First barrier layer
	34	Second barrier layer
	35	Third barrier layer
	40	Chip formation region (Device formation region)
10	41	Scribe region
	42	Substrate
	43A	Multi-layered structure
	43B	Protection oxide film
	43C	Protection oxide film
15	44	Insulating film
	50	Device formation region
	51	Pad electrode formation region
	52	Substrate
	53A	Multi-layered structure
20	53B	Insulating oxide film
	54	Pad electrode
	60A	Laser structure
	60	Laser structure formation region
	60a	Emitting facet
25	60b	Reflecting facet

	61	Substrate
	62	N-type contact layer
	63	N-type cladding layer
	64	Active layer
5	65	P-type cladding layer
	66	P-type contact layer
	67	P-side electrode
	67A	P-side electrode formation region
	68	N-side electrode
10	68A	N-side electrode formation region
	70	Protection oxide film

[Name of the Document] ABSTRACT

[Summary]

[Purpose]

The invention aims at the formation of an insulating
5 film having high adhesion to a group III nitride
semiconductor, a good electric characteristic or a good
optical characteristic.

[Means of Solving]

The semiconductor device of this invention includes an
10 active region **12A** of SiC grown on a substrate **11** and an
insulating oxide film **12B** formed in a peripheral portion of
the active region **12A** by oxidizing the group III nitride
semiconductor. On the active region **12A**, a gate electrode **13**
in Schottky contact with the active region **12A** extending onto
15 the insulating oxide film **12B** and having an extended portion
13a on the insulating oxide film **12B** is formed, and ohmic
electrodes **14** respectively serving as a source electrode and
a drain electrode are formed with space from side edges along
the gate length direction of the gate electrode **13**.

20 [Selected figure] FIG. 1

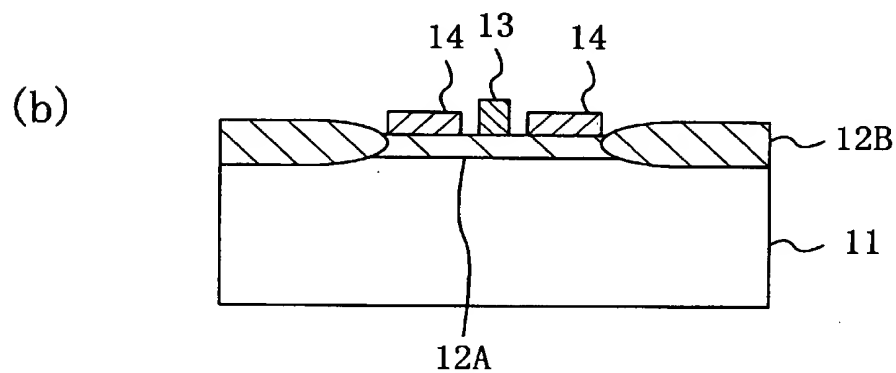
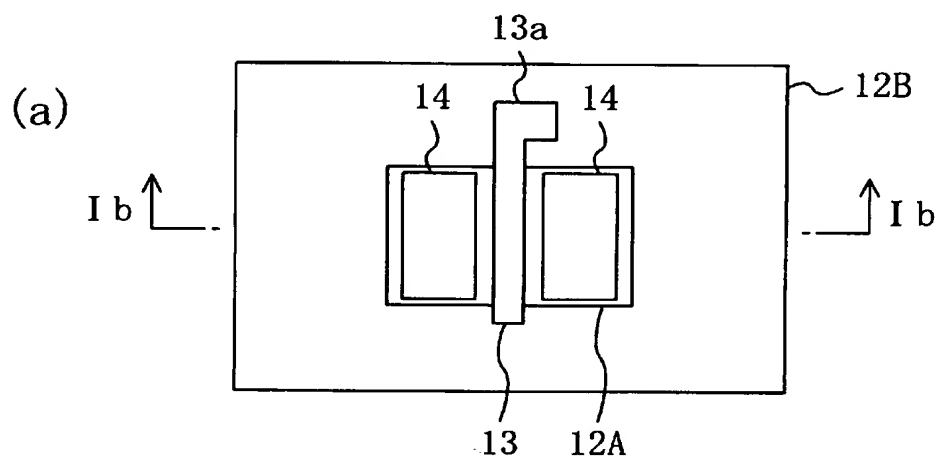


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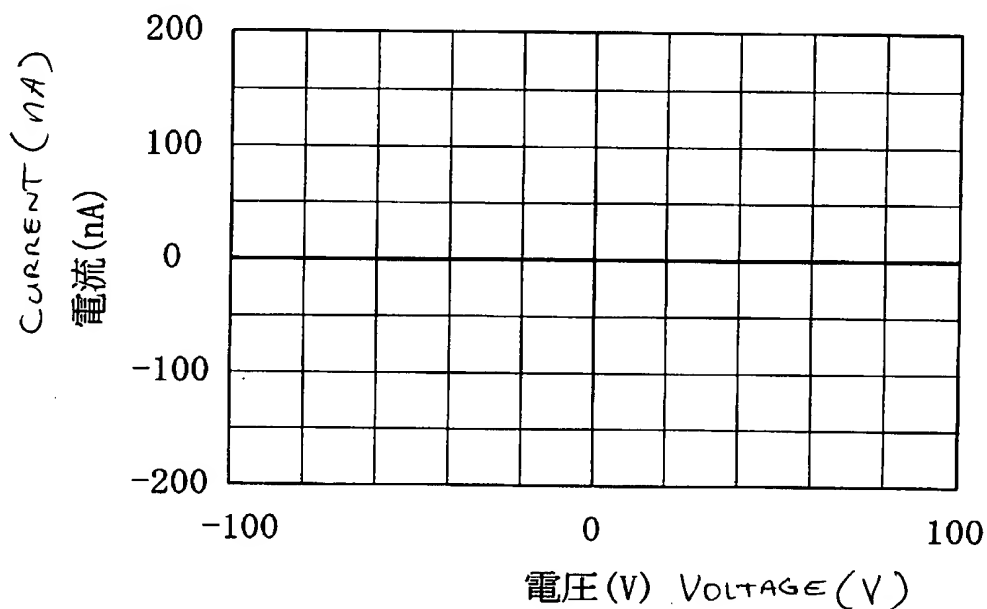
【書類名】 図面 [Name of the Document] DRAWINGS

【図1】 [FIG. 1]

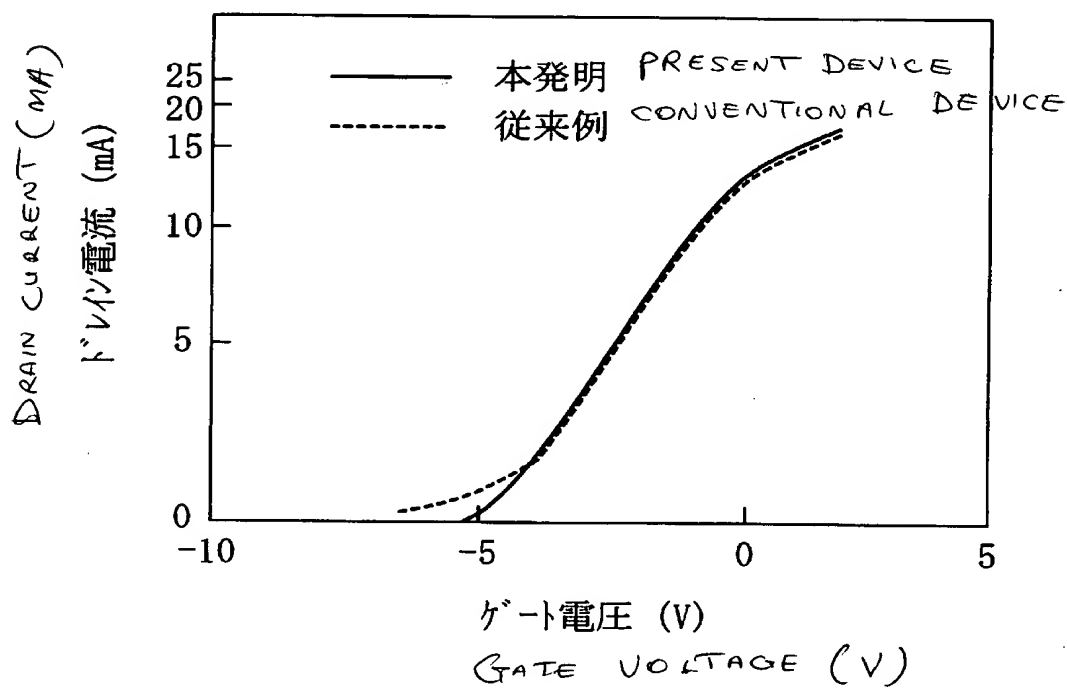




【図2】 [FIG. 2]



【図3】 [FIG. 3]



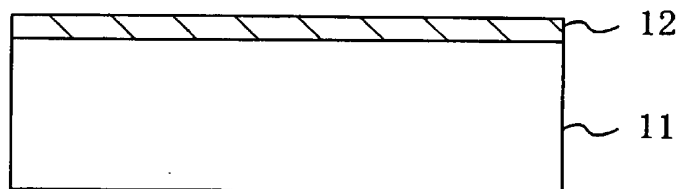


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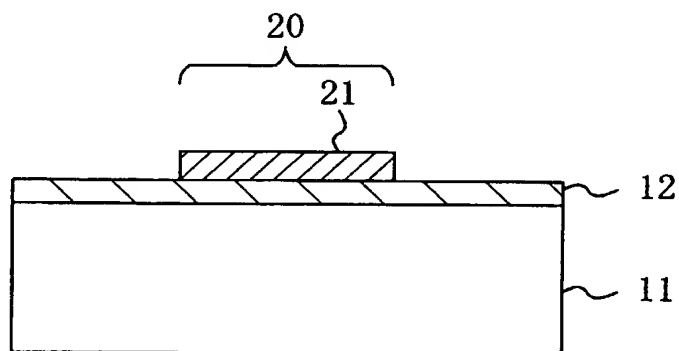
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【図4】 [FIG. 4]

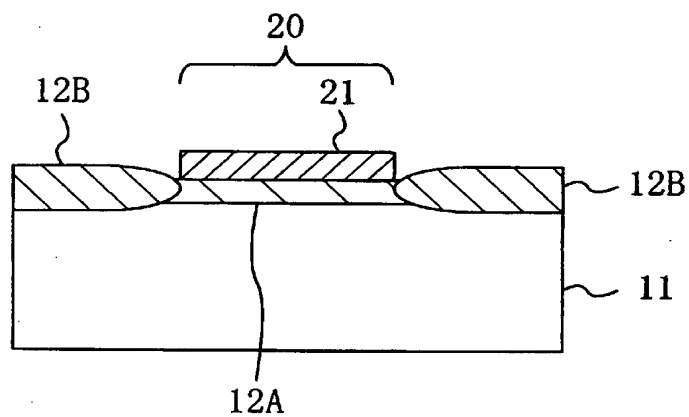
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(b)

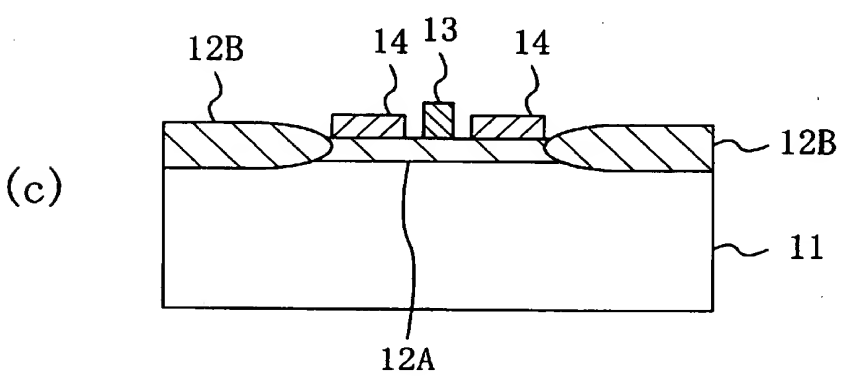
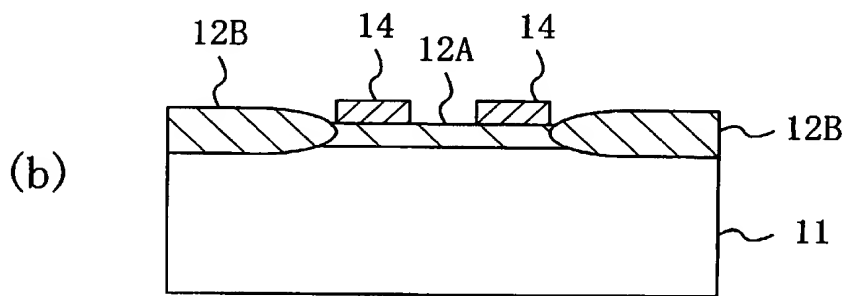
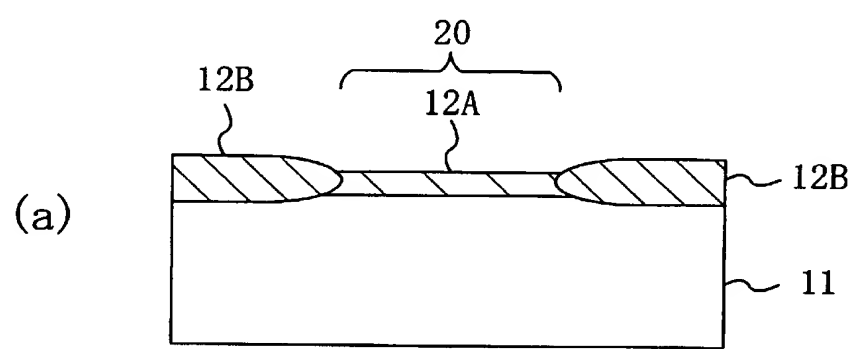


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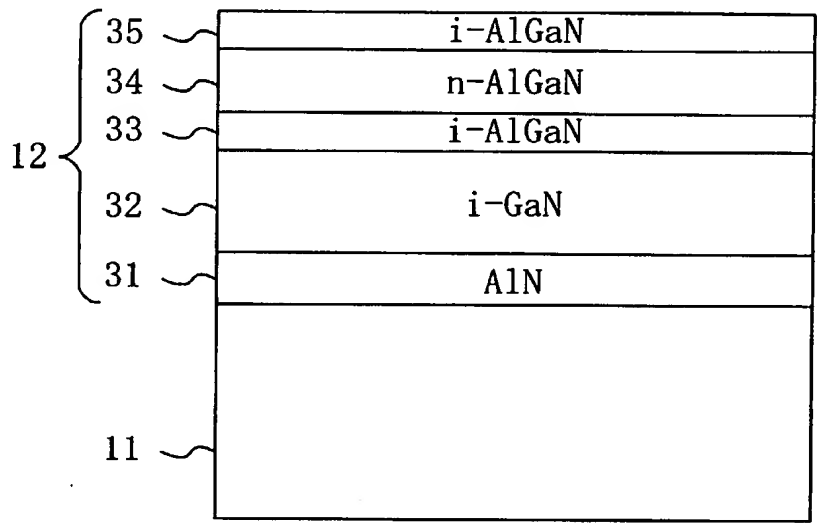


【図5】 [FIG. 5]

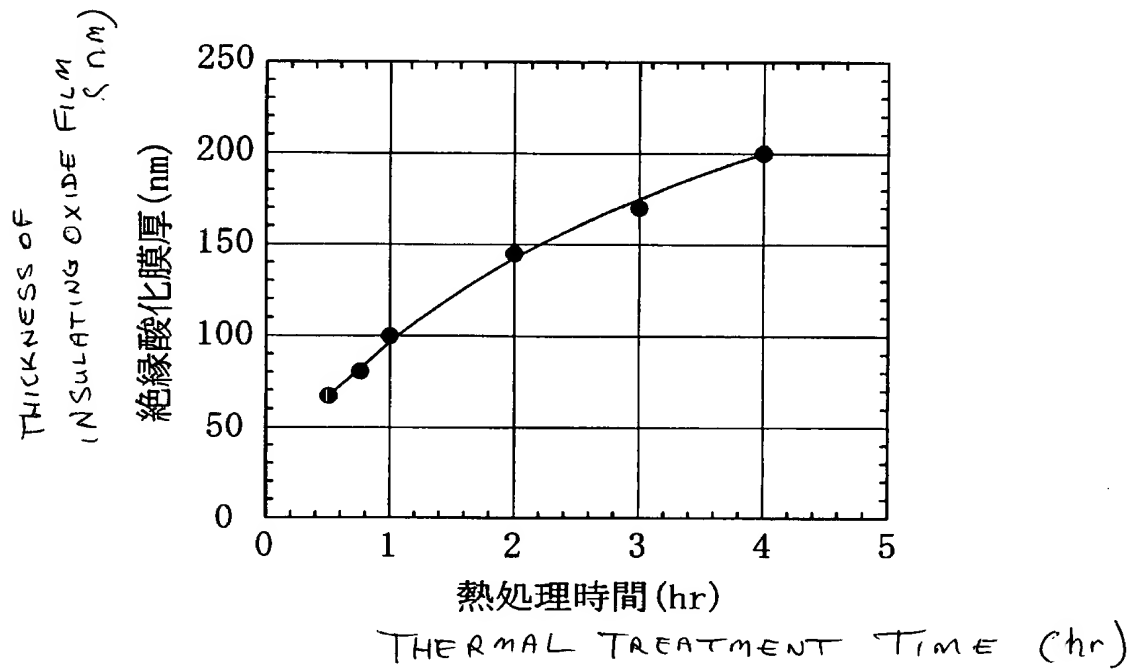




【図6】 [FIG. 6]



【図7】 [FIG. 7]

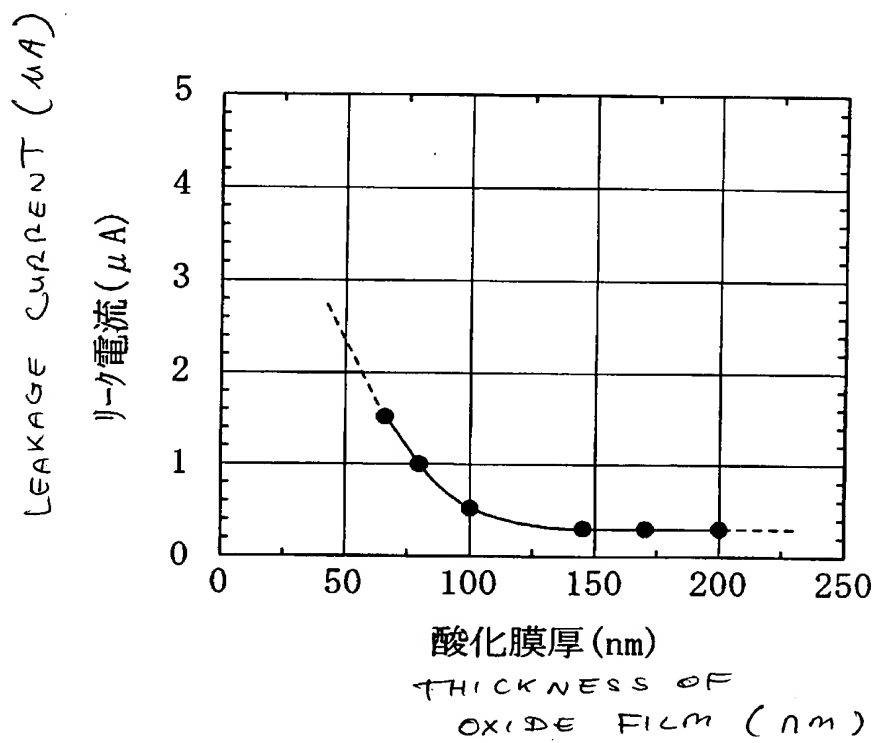




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【図8】 [FIG. 8]

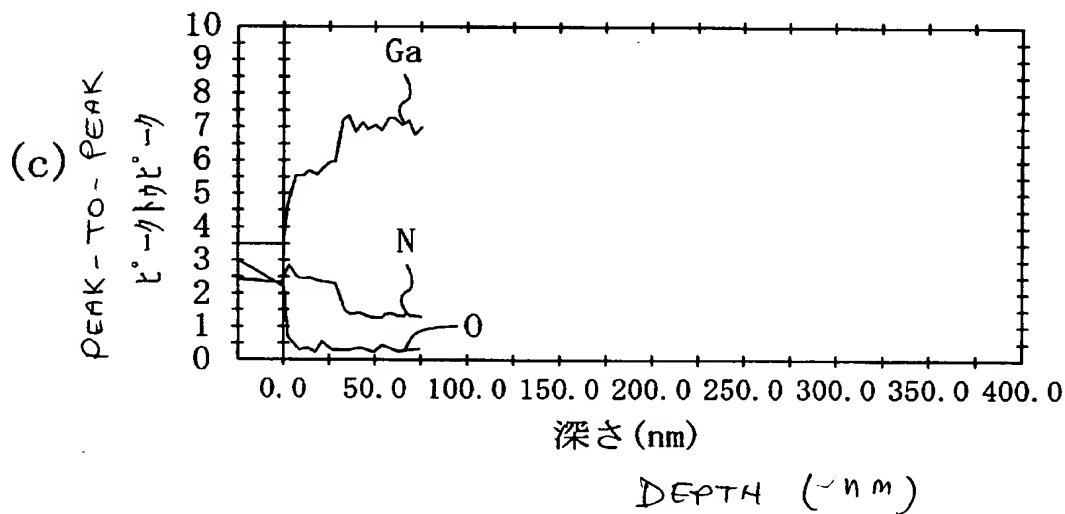
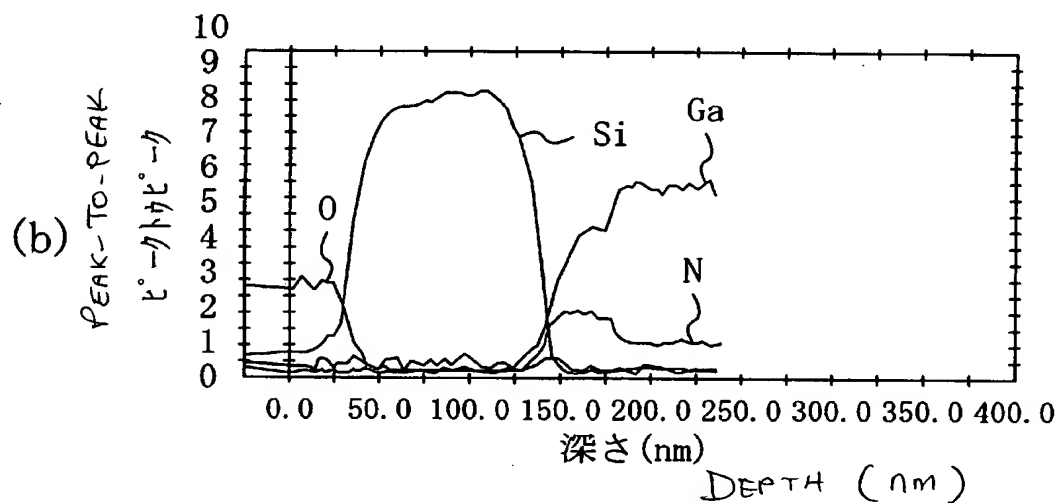
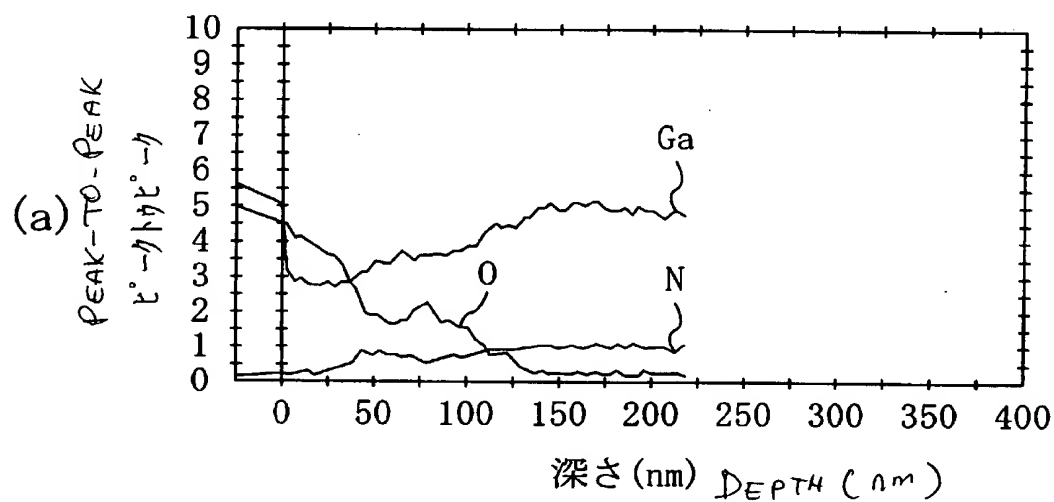




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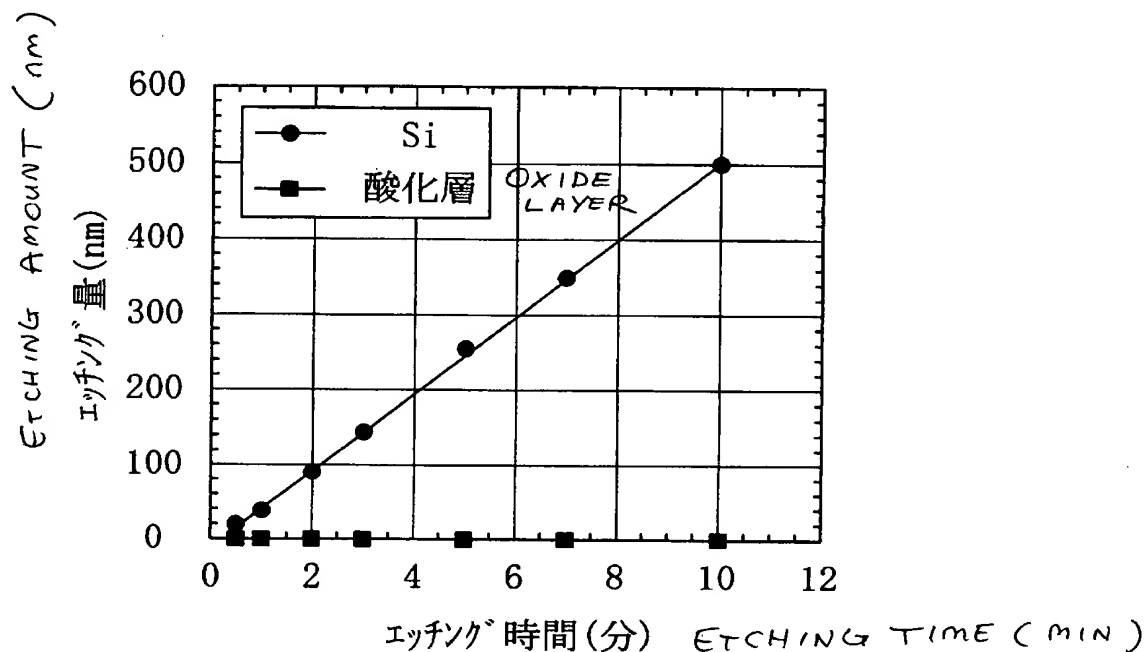
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【図9】 [FIG. 9]

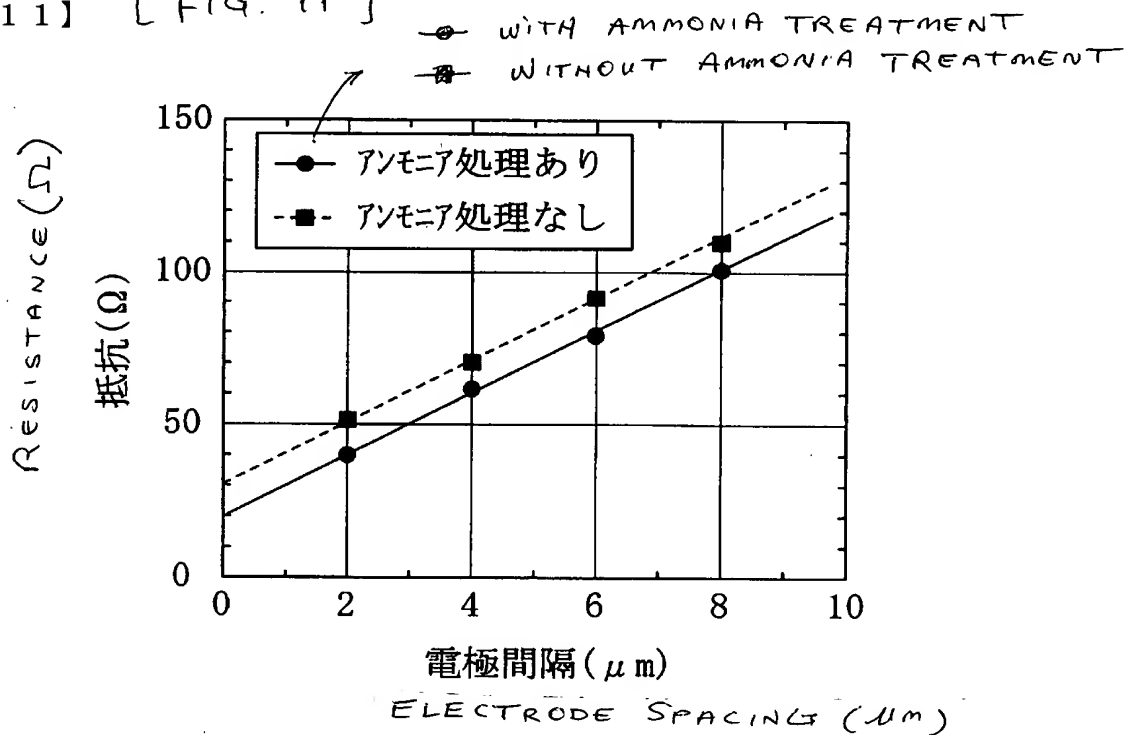




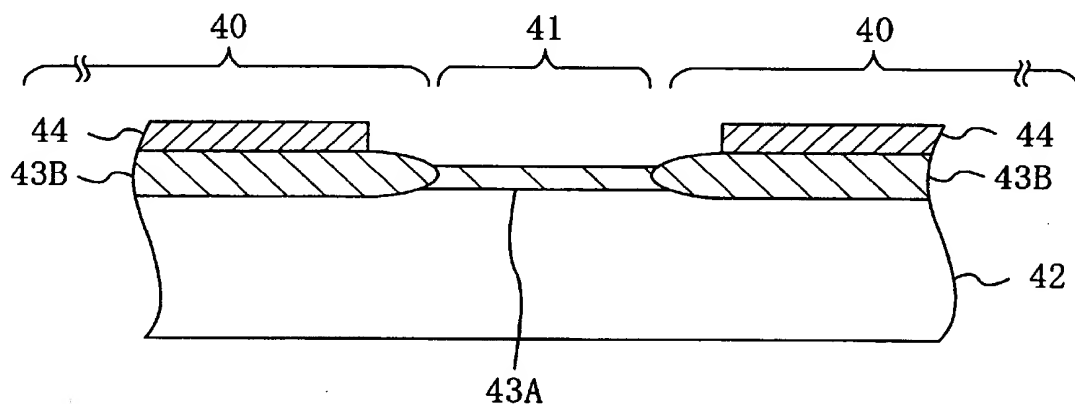
【図10】 [FIG. 10]



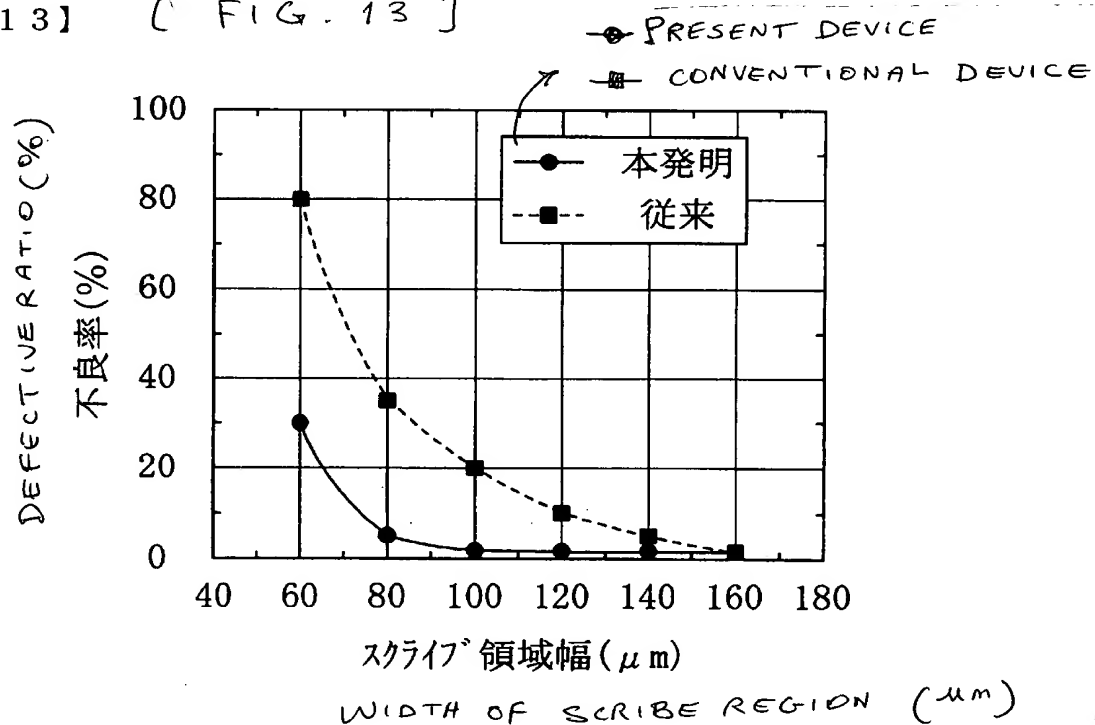
【図11】 [FIG. 11]



【図12】 [FIG. 12]



【図13】 [FIG. 13]

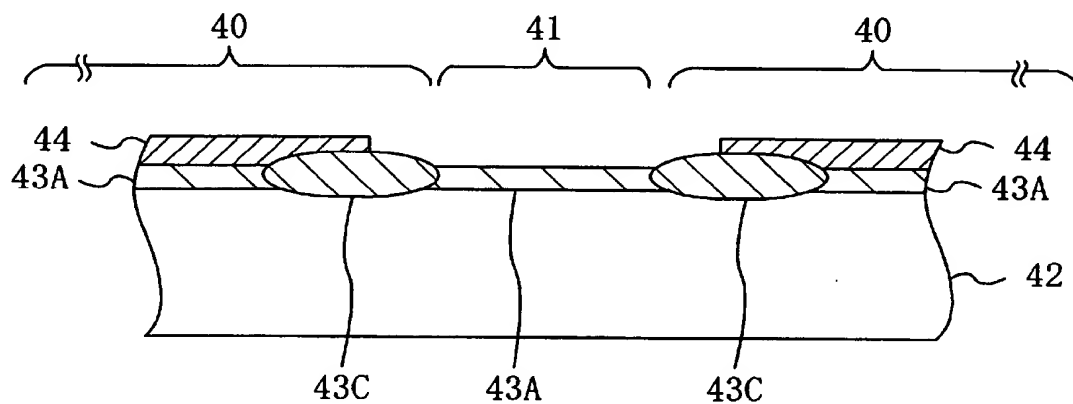




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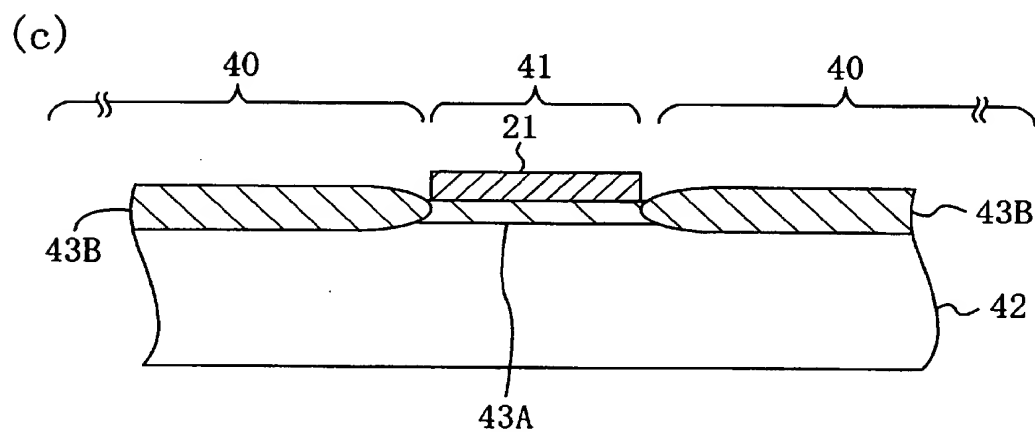
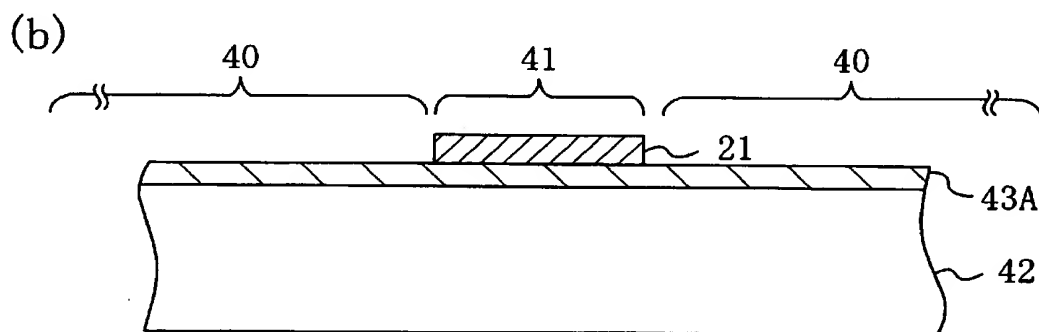
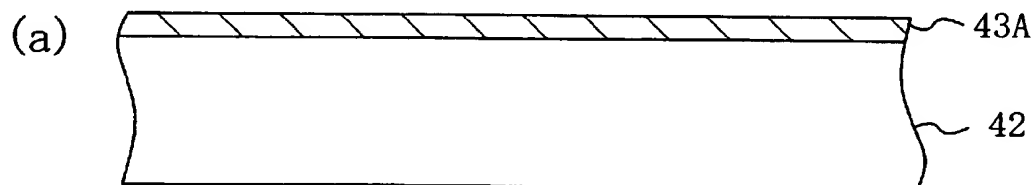
【図14】 [FIG. 14]





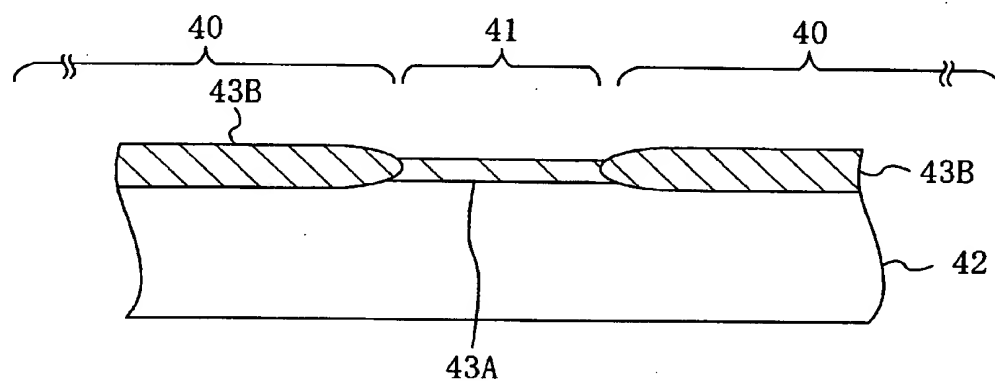
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【図15】 [FIG. 15]

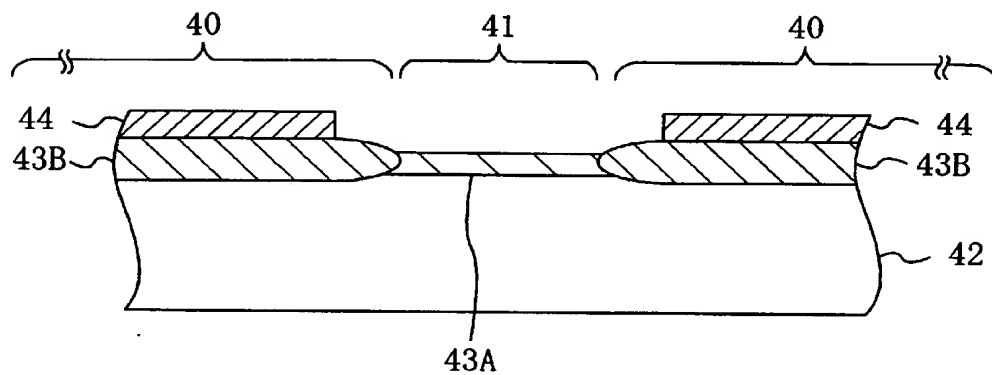


【図16】 [FIG. 16]

(a)



(b)

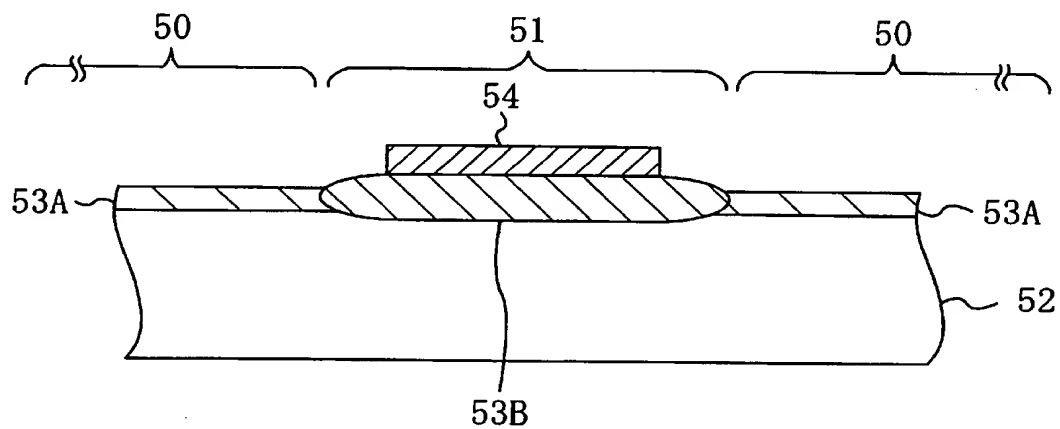




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【図17】 [FIG. 17]

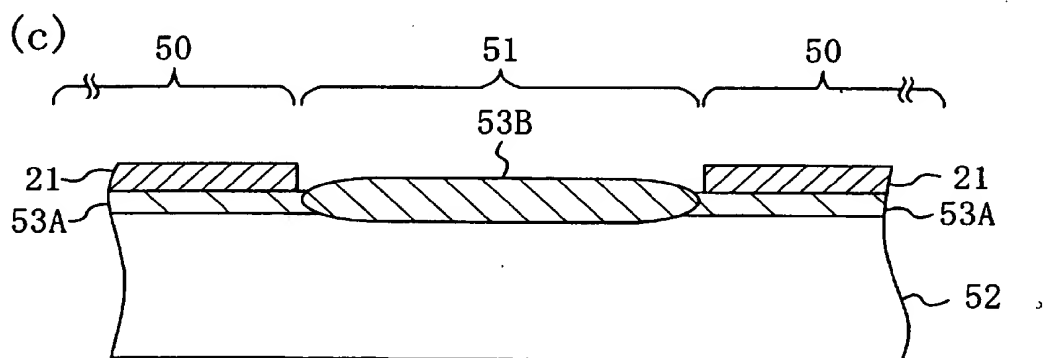
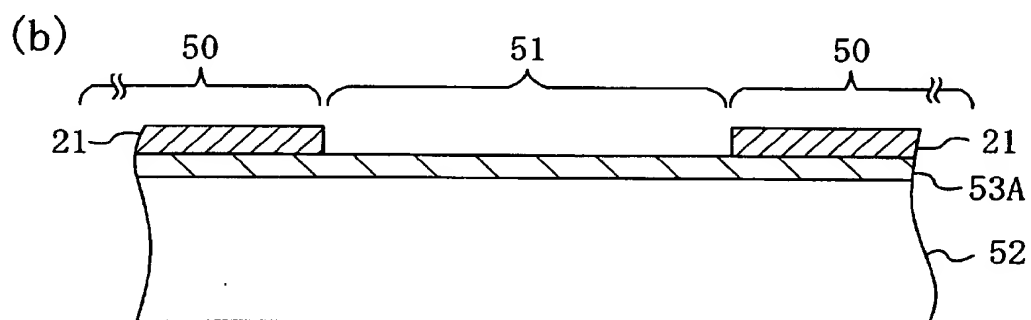
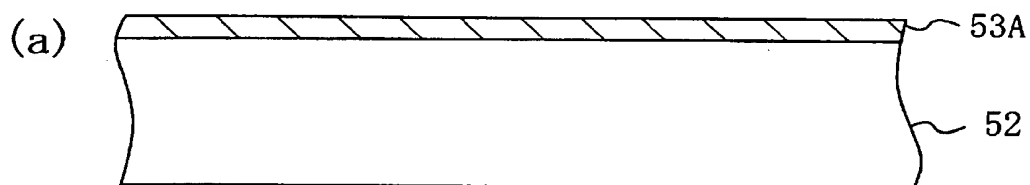




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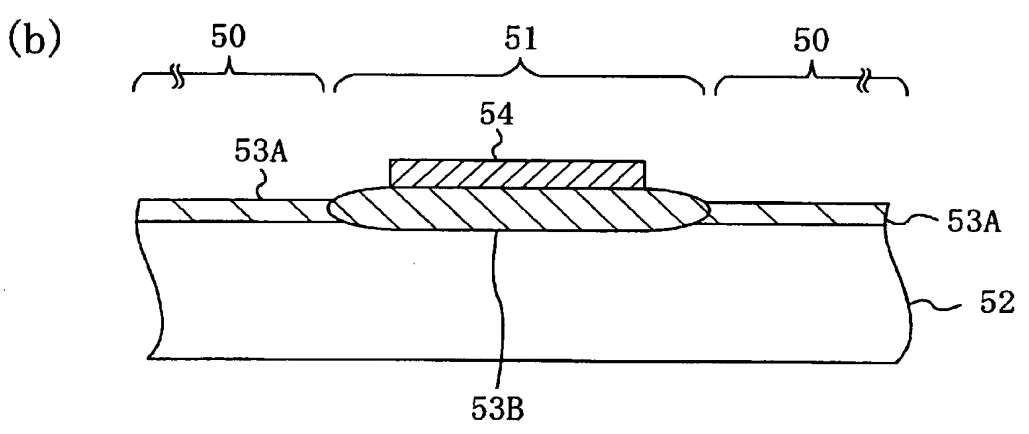
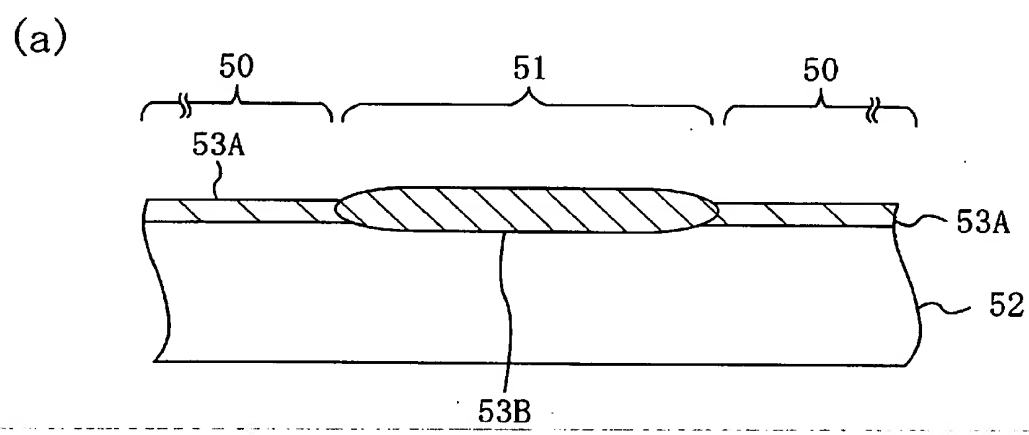
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【図18】 [FIG. 18]





【図19】 [FIG. 19]

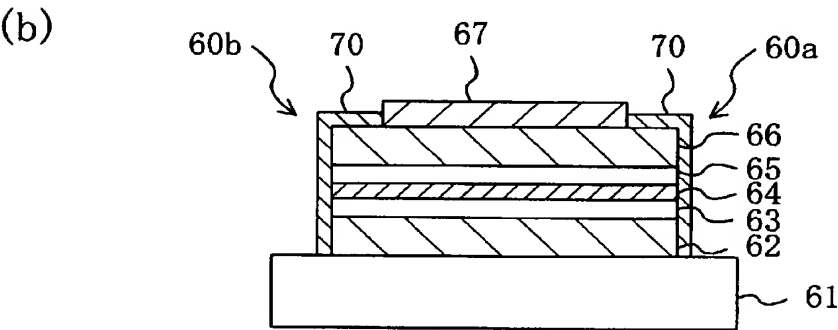
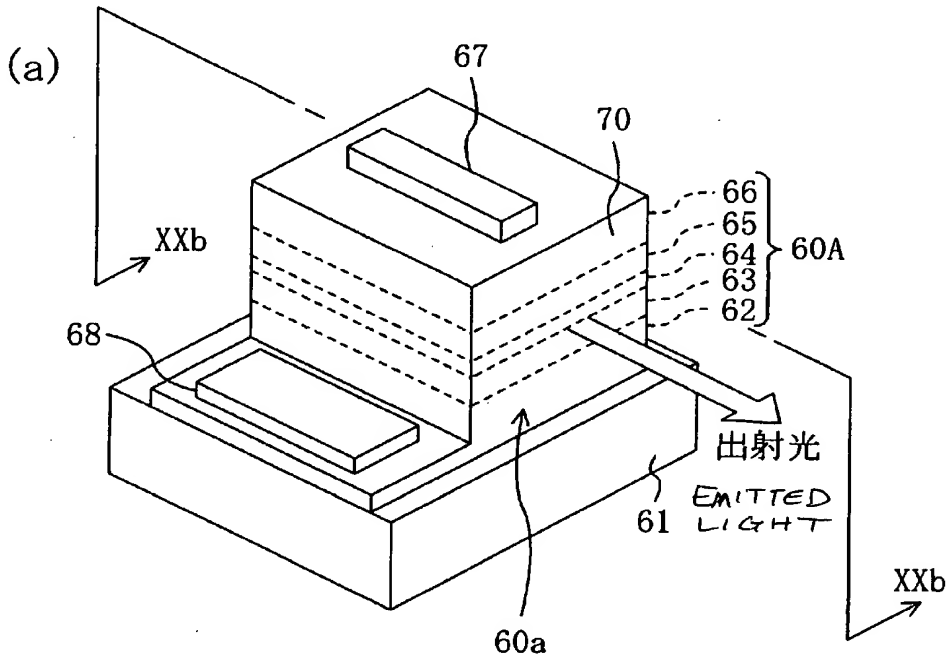




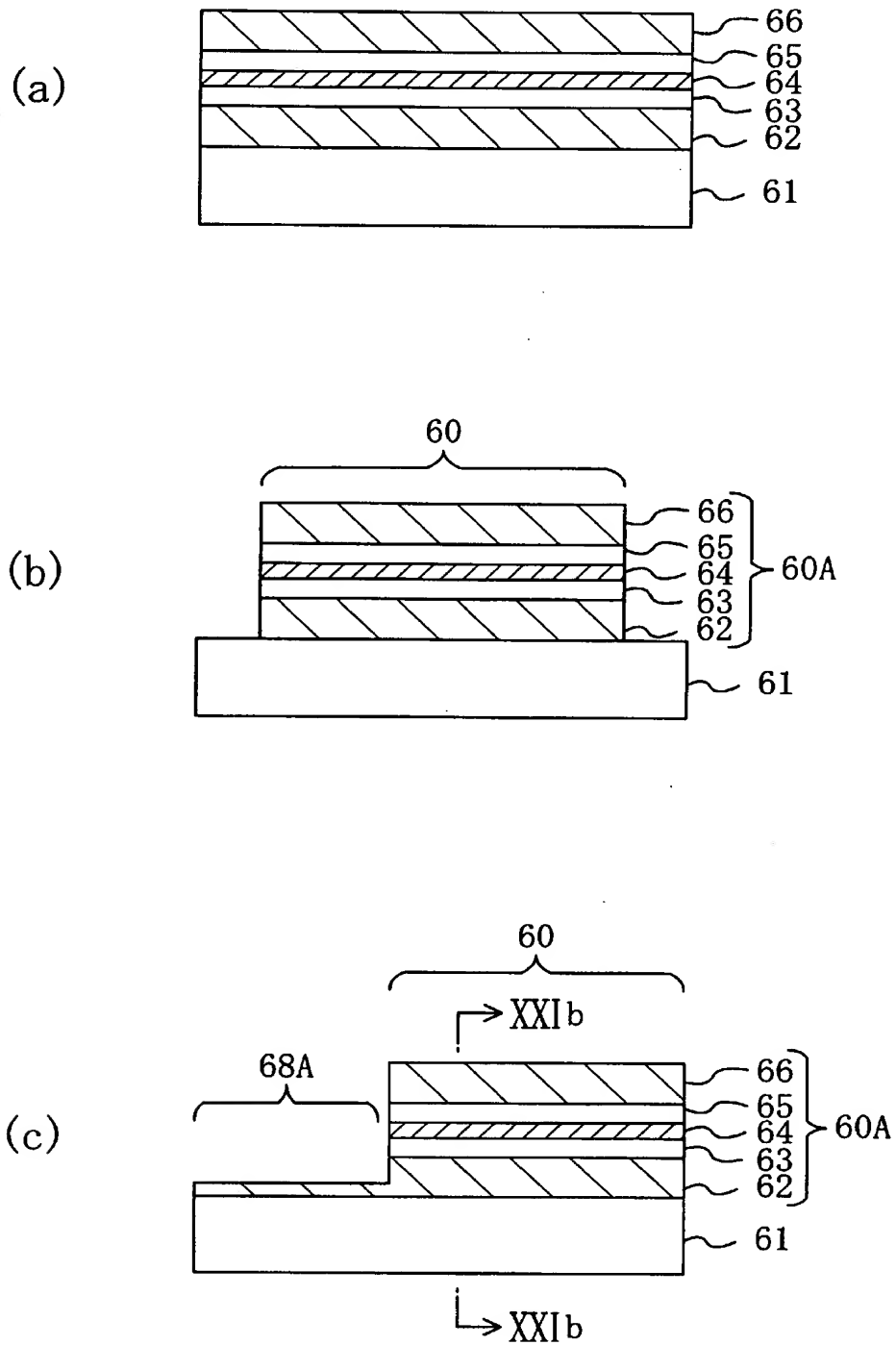
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【図20】 [FIG. 20]



【図21】 [FIG. 21]

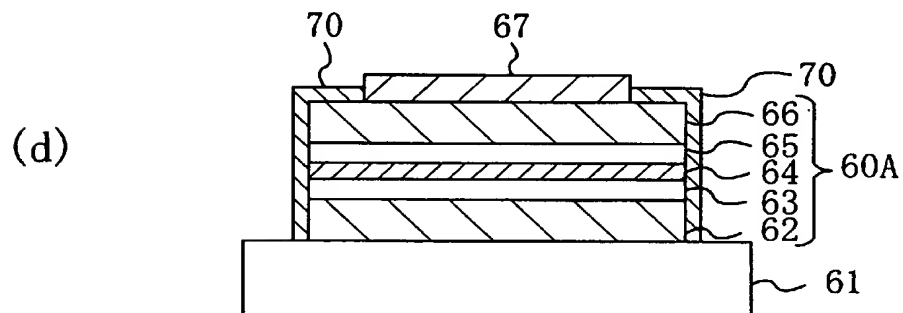
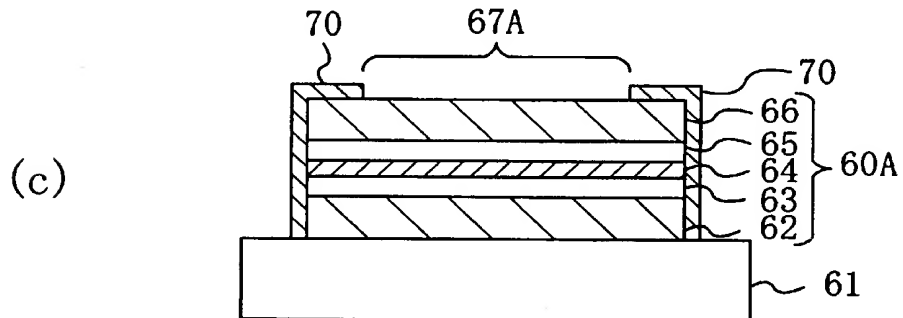
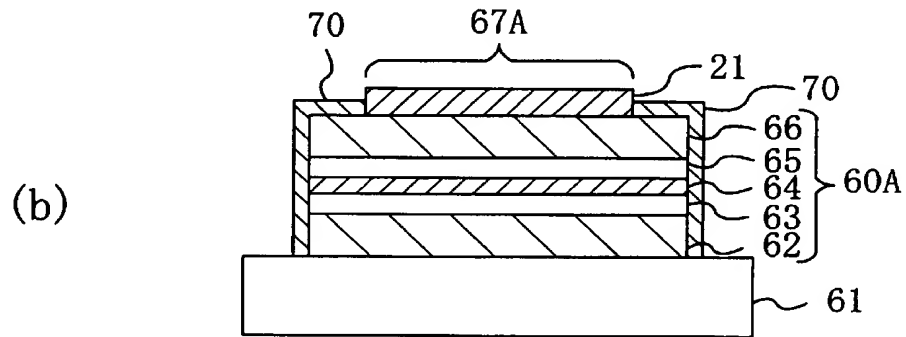
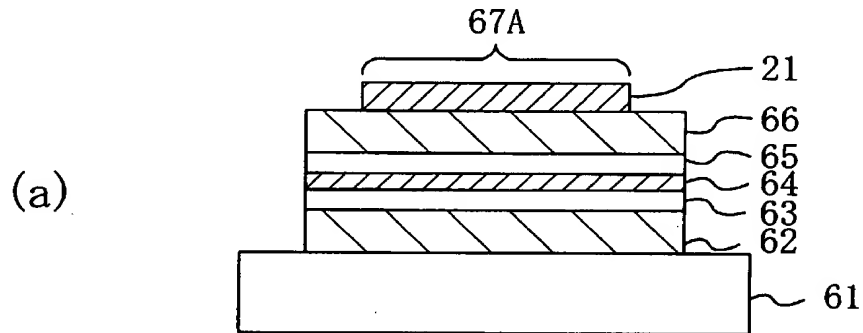




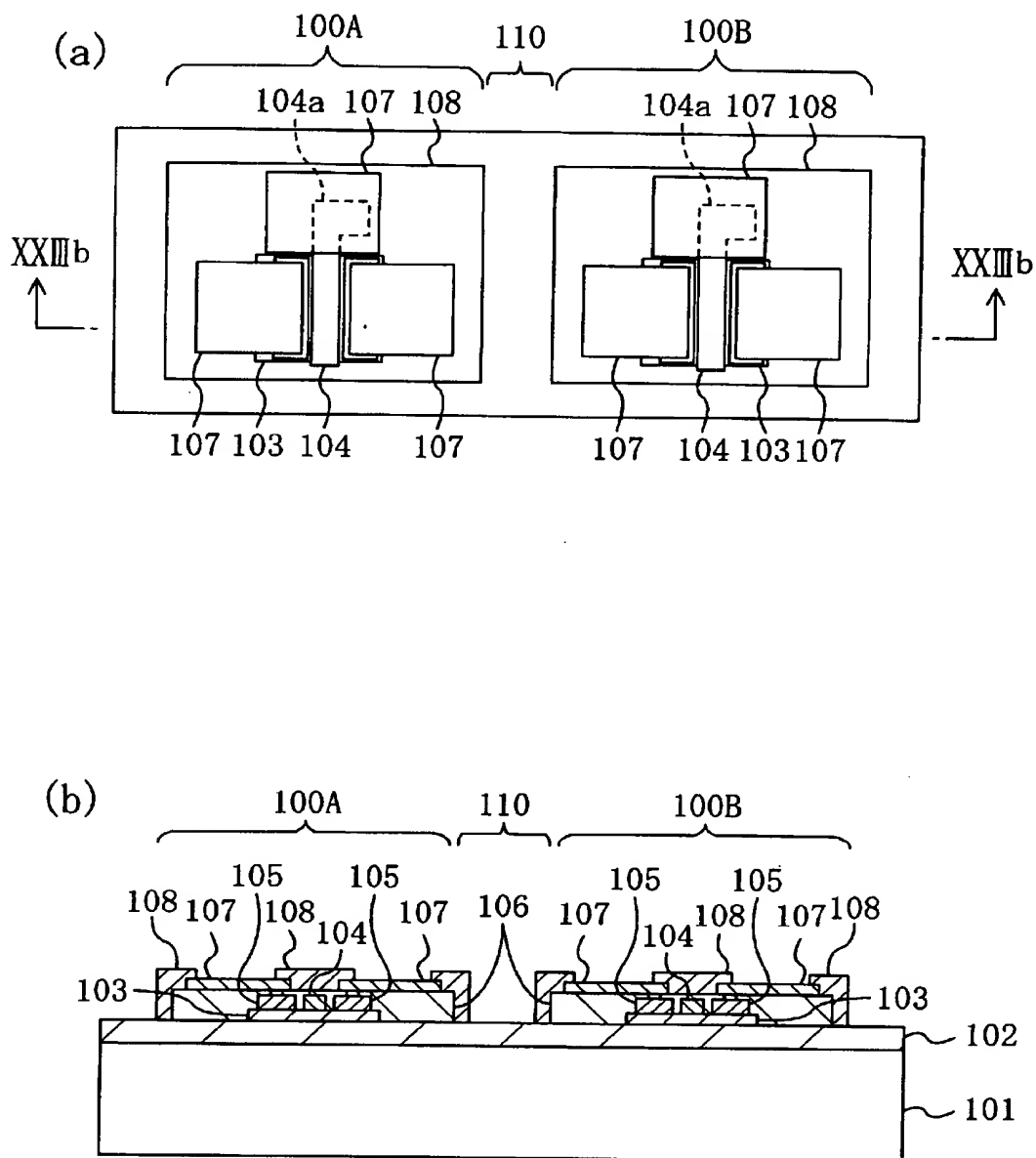
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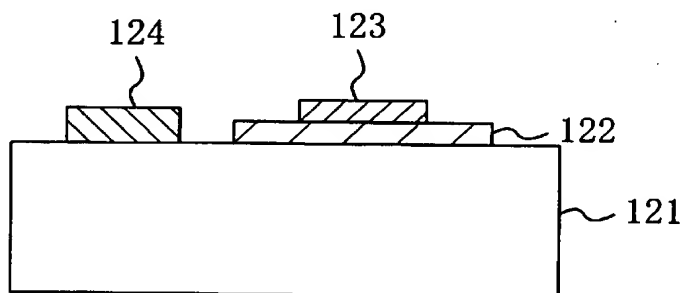
【図22】 [FIG. 22]



【図 23】 [FIG. 23]



【図24】 [FIG. 24]



【図25】 [FIG. 25]

